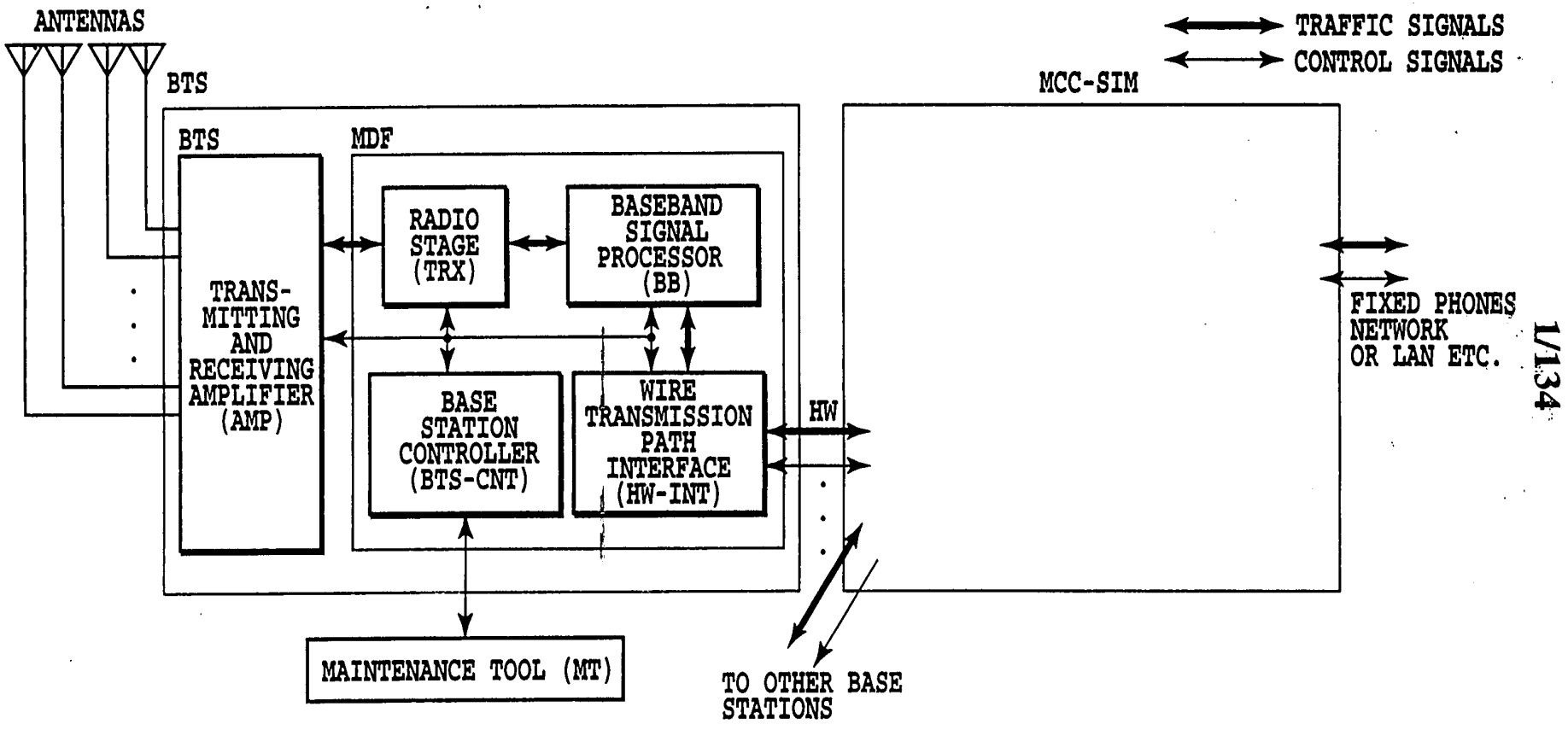

ANTENNAS
BTS
BTS
MDF
TRANS-
MITTING
AND
RECEIVING
AMPLIFIER
(AMP)
RADIO
STAGE
(TRX)
BASEBAND
SIGNAL
PROCESSOR
(BB)
BASE
STATION
CONTROLLER
(BTS-CNT)
WIRE
TRANSMISSION
PATH
INTERFACE
(HW-INT)
HW
MAINTENANCE TOOL (MT)
TO OTHER BASE
STATIONS
MCC-SIM
TRAFFIC SIGNALS
CONTROL SIGNALS
FIXED PHONES
NETWORK
OR LAN ETC.

FIG.1

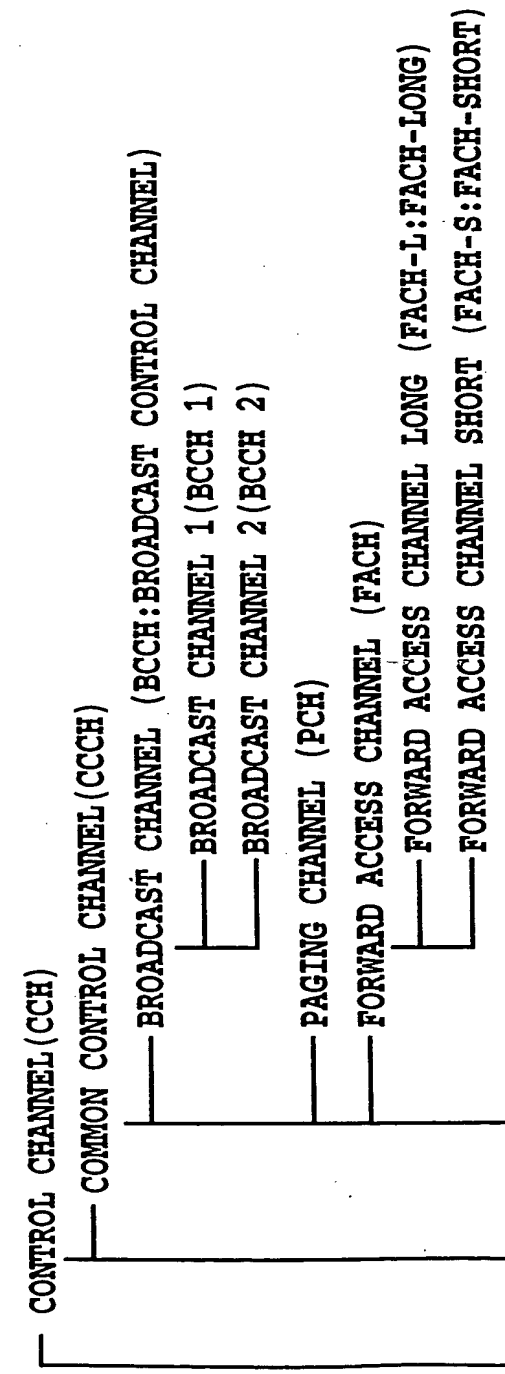

CONTROL CHANNEL(CCH)
COMMON CONTROL CHANNEL(CCCH)
BROADCAST CHANNEL (BCCH:BROADCAST CONTROL CHANNEL)
BROADCAST CHANNEL 1(BCCH 1)
BROADCAST CHANNEL 2(BCCH 2)
PAGING CHANNEL (PCH)
FORWARD ACCESS CHANNEL (FACH)
FORWARD ACCESS CHANNEL LONG (FACH-L:FACH-LONG)
FORWARD ACCESS CHANNEL SHORT (FACH-S:FACH-SHORT)
RANDOM ACCESS CHANNEL (RACH)
RANDOM ACCESS CHANNEL LONG(RACH-L:RACH-LONG)
RANDOM ACCESS CHANNEL SHORT(RACH-S:RACH-SHORT)
DEDICATED CONTROL CHANNEL(DCCH)
STAND ALONE DEDICATED CONTROL CHANNEL(SDCCH)
ASSOCIATED CONTROL CHANNEL(ACCH)
TRAFFIC CHANNEL(TCH)
DEDICATED TRAFFIC CHANNEL(DTCH)
USER PACKET CHANNEL(UPCH)

FIG.2

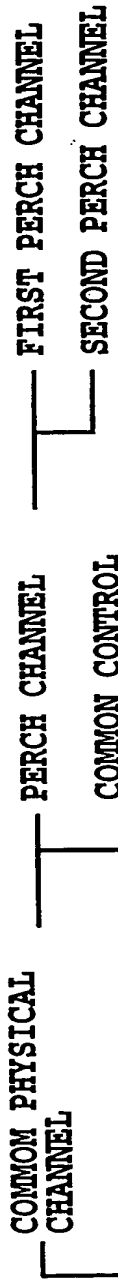

COMMON PHYSICAL CHANNEL
DEDICATED PHYSICAL CHANNEL
PERCH CHANNEL
COMMON CONTROL PHYSICAL CHANNEL
FIRST PERCH CHANNEL
SECOND PERCH CHANNEL

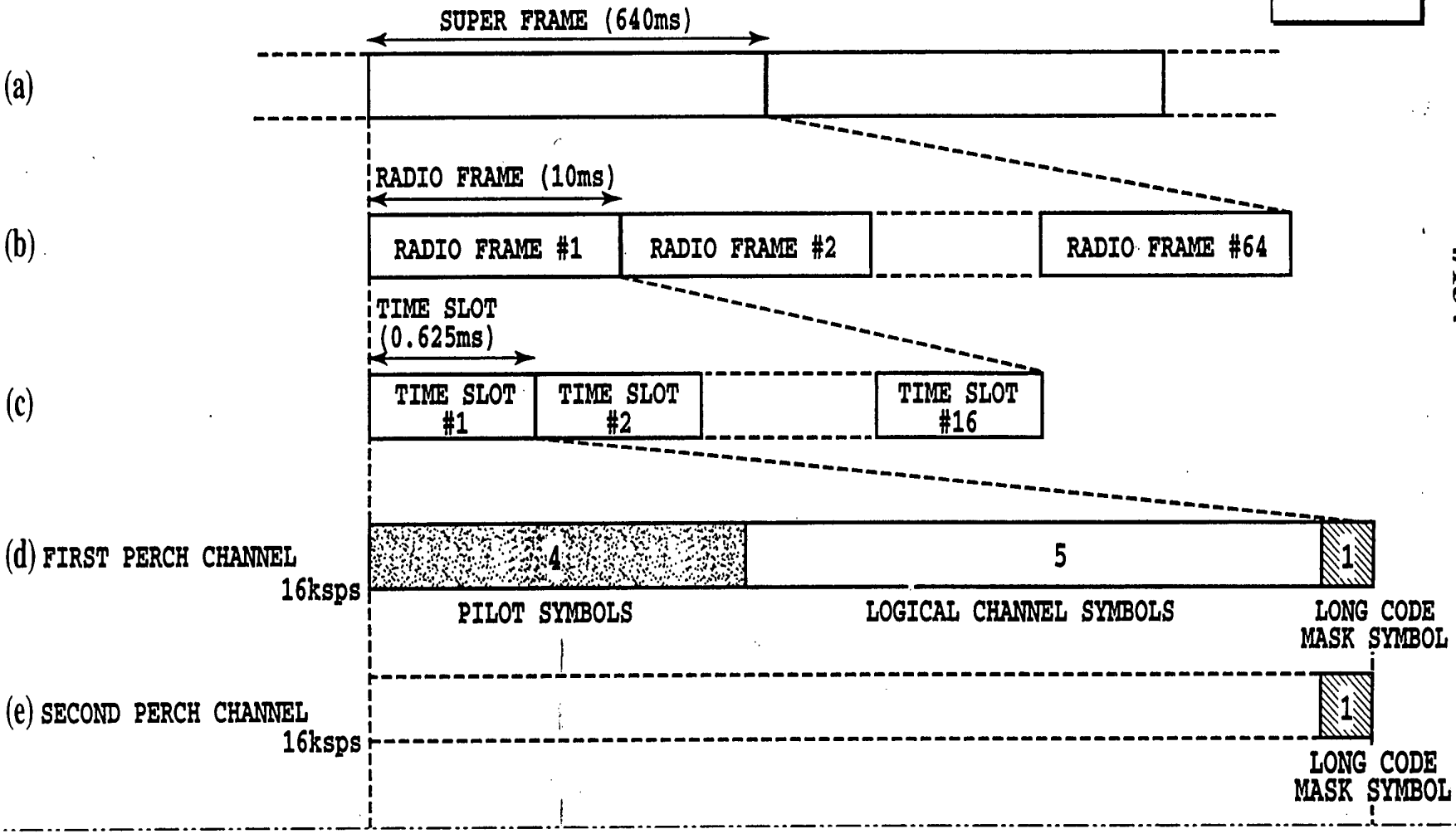
FIG.3

FIG.4

FIG.4A

FIG.4B

FIG.4A



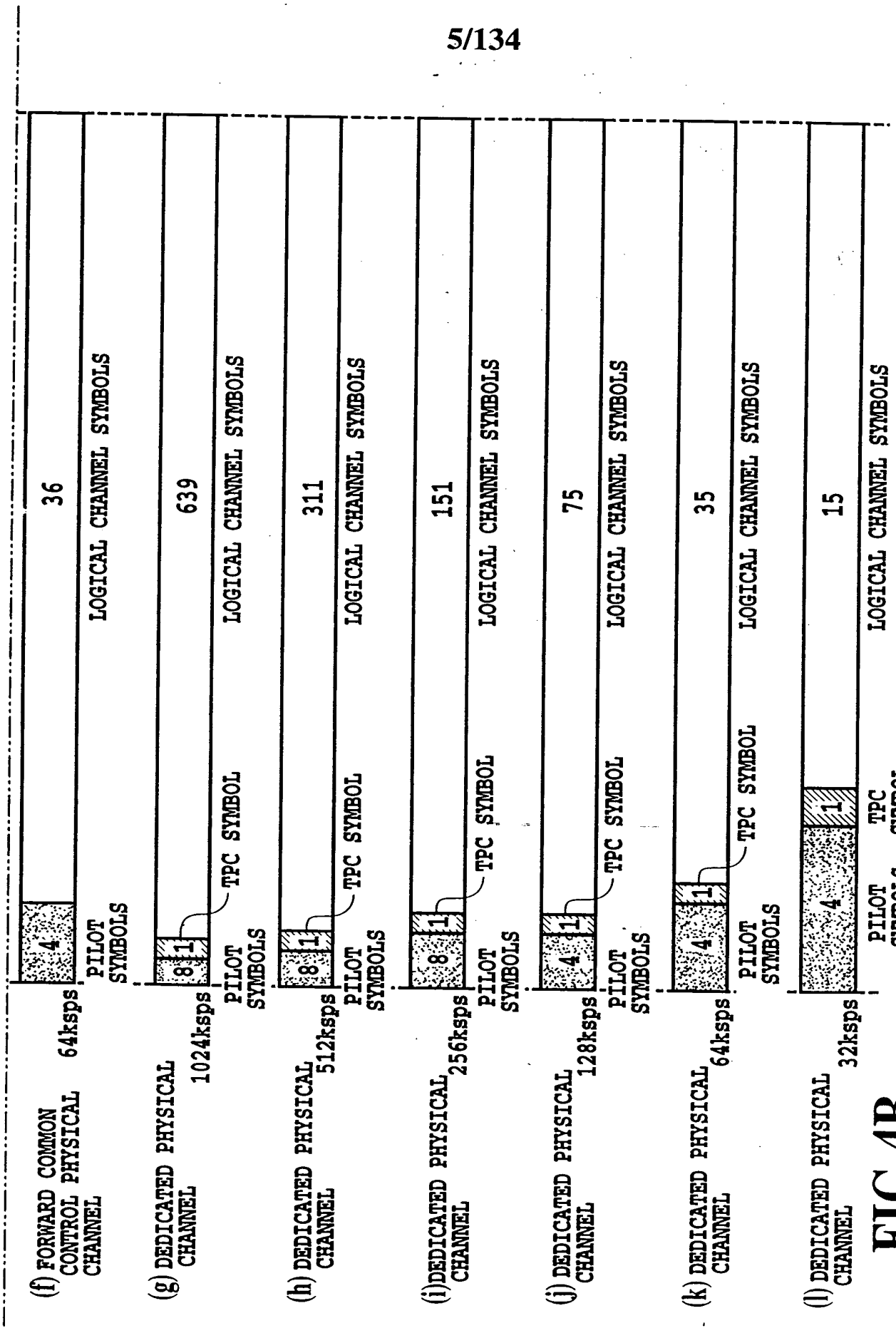

(f) FORWARD COMMON CONTROL PHYSICAL CHANNEL
64ksps
4
36
PILOT SYMBOLS
LOGICAL CHANNEL SYMBOLS
(g) DEDICATED PHYSICAL CHANNEL
1024ksps
8
1
639
PILOT SYMBOLS
TPC SYMBOL
LOGICAL CHANNEL SYMBOLS
(h) DEDICATED PHYSICAL CHANNEL
512ksps
8
1
311
PILOT SYMBOLS
TPC SYMBOL
LOGICAL CHANNEL SYMBOLS
(i) DEDICATED PHYSICAL CHANNEL
256ksps
8
1
151
PILOT SYMBOLS
TPC SYMBOL
LOGICAL CHANNEL SYMBOLS
(j) DEDICATED PHYSICAL CHANNEL
128ksps
4
1
75
PILOT SYMBOLS
TPC SYMBOL
LOGICAL CHANNEL SYMBOLS
(k) DEDICATED PHYSICAL CHANNEL
64ksps
4
1
35
PILOT SYMBOLS
TPC SYMBOL
LOGICAL CHANNEL SYMBOLS
(l) DEDICATED PHYSICAL CHANNEL
32ksps
4
1
15
PILOT SYMBOLS
TPC SYMBOL
LOGICAL CHANNEL SYMBOLS

FIG.4B

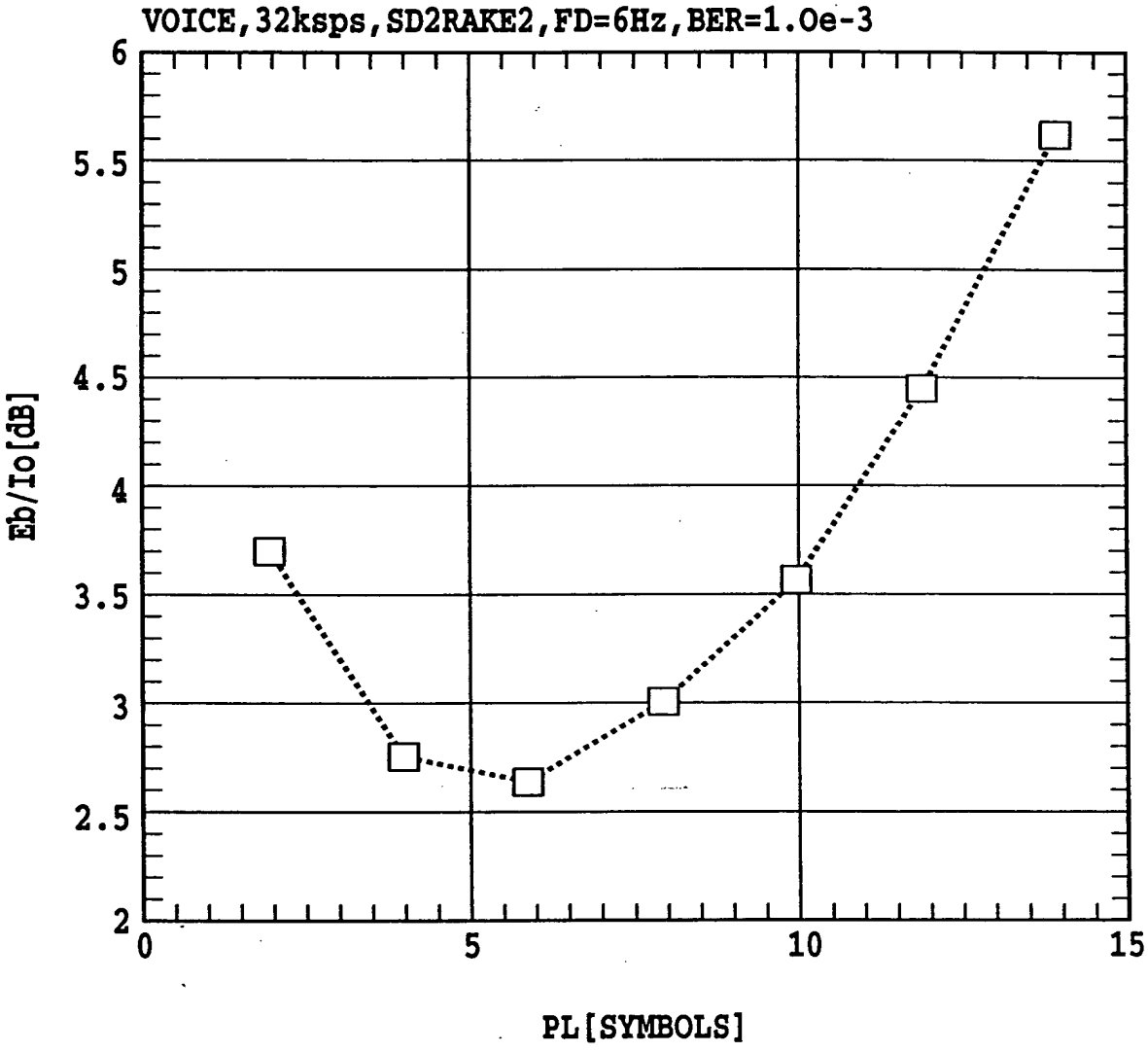

VOICE,32ksps,SD2RAKE2,FD=6Hz,BER=1.0e-3
Eb/Io[dB]
6
5.5
5
4.5
4
3.5
3
2.5
2
0
5
10
15
PL[SYMBOLS]

FIG.5

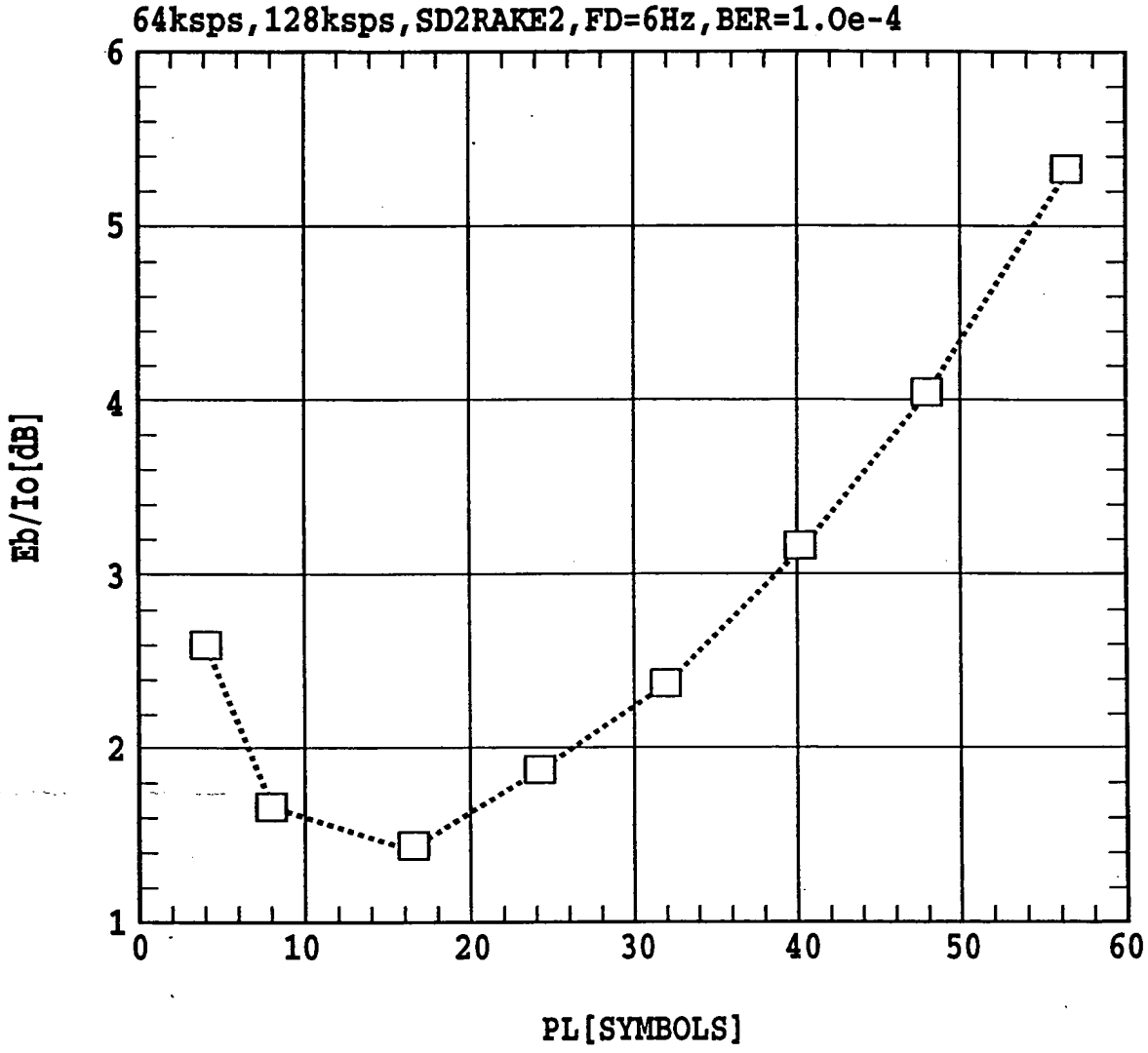

64ksps,128ksps,SD2RAKE2,FD=6Hz,BER=1.0e-4
Eb/Io[dB]
PL[SYMBOLS]
1
2
3
4
5
6
0
10
20
30
40
50
60

FIG.6

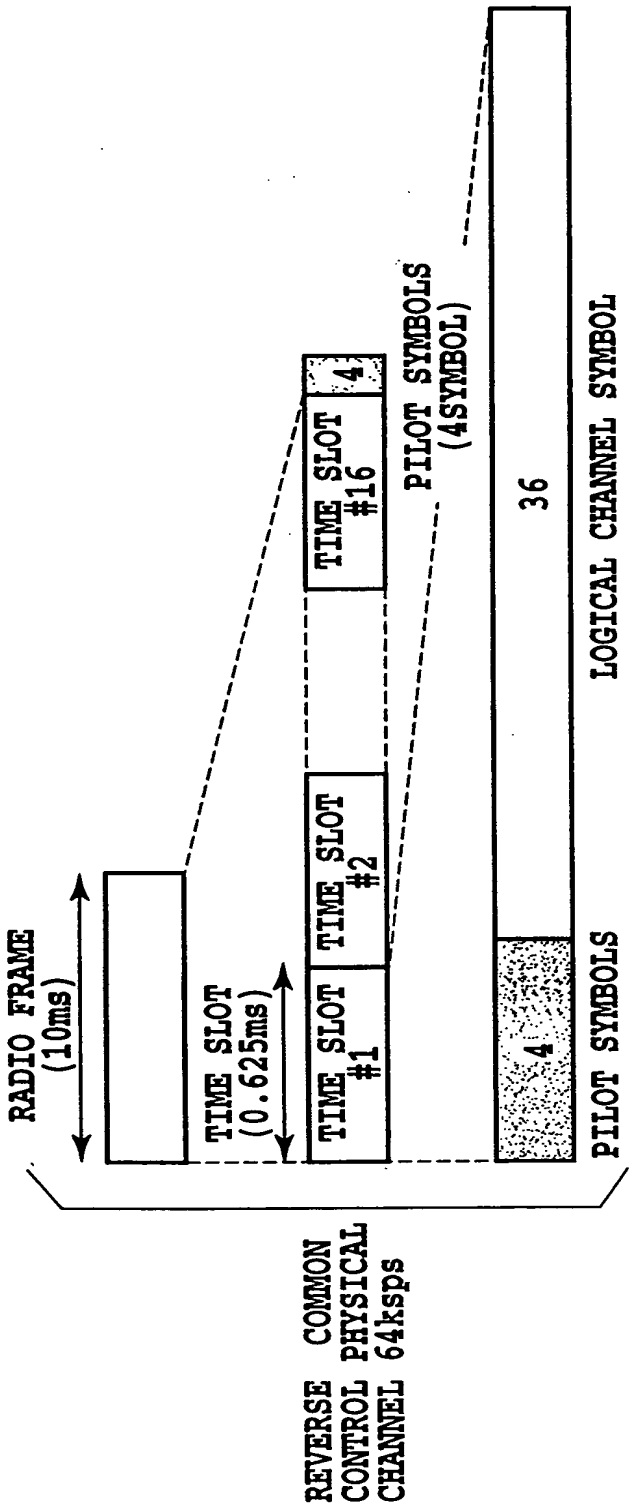

RADIO FRAME
(10ms)
TIME SLOT
(0.625ms)
TIME SLOT #1
TIME SLOT #2
TIME SLOT #16
4
PILOT SYMBOLS
(4SYMBOL)
36
4
LOGICAL CHANNEL SYMBOL
PILOT SYMBOLS
REVERSE COMMON CONTROL PHYSICAL CHANNEL 64ksps

FIG.7A

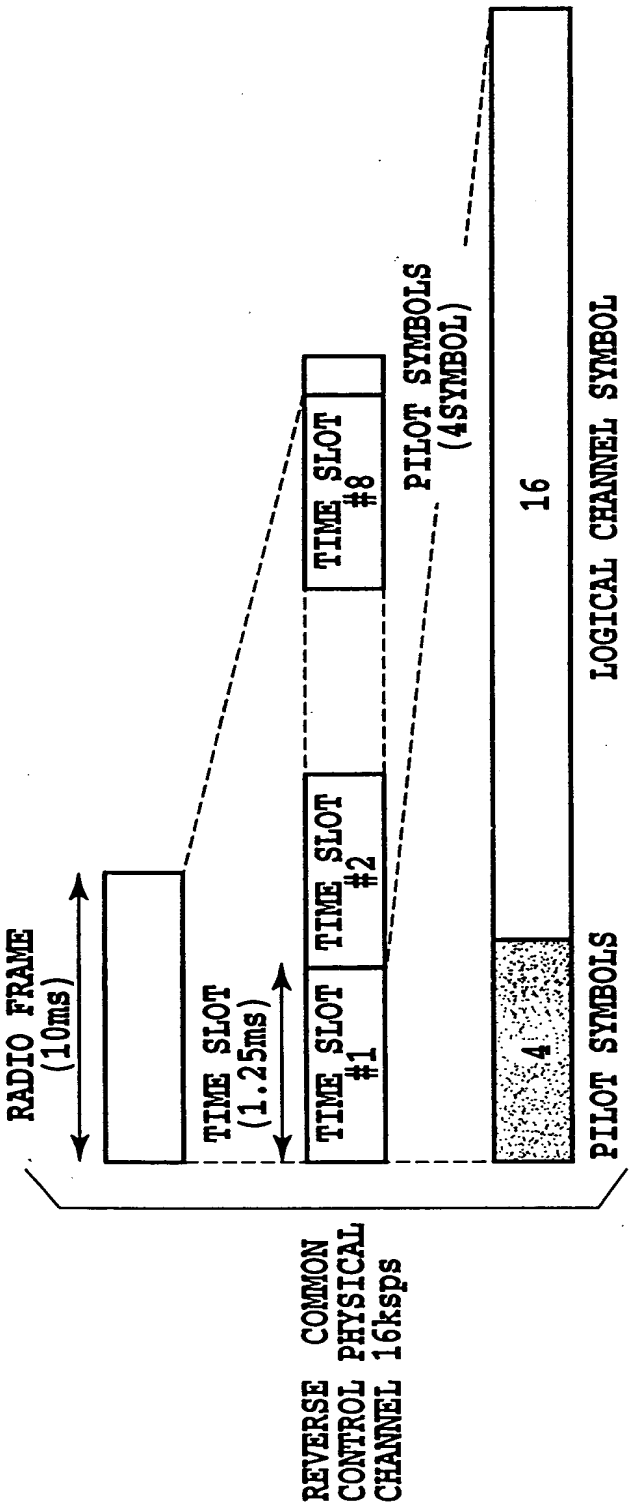

REVERSE COMMON CONTROL PHYSICAL CHANNEL 16ksps
RADIO FRAME (10ms)
TIME SLOT (1.25ms)
TIME SLOT #1
TIME SLOT #2
TIME SLOT #8
PILOT SYMBOLS (4SYMBOL)
16
4
LOGICAL CHANNEL SYMBOL
PILOT SYMBOLS

FIG.7B

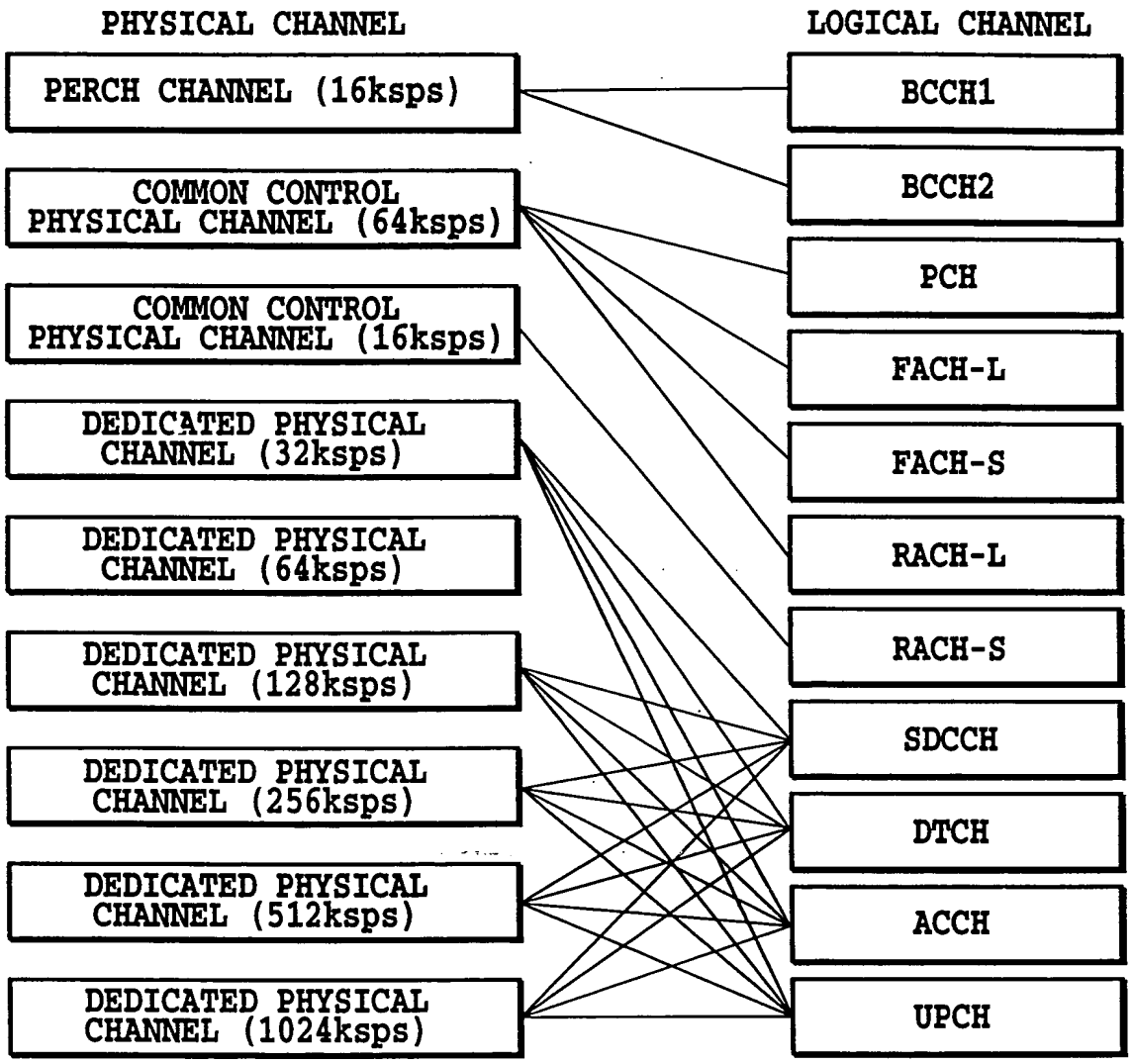

PHYSICAL CHANNEL
LOGICAL CHANNEL
PERCH CHANNEL (16ksps)
COMMON CONTROL PHYSICAL CHANNEL (64ksps)
COMMON CONTROL PHYSICAL CHANNEL (16ksps)
DEDICATED PHYSICAL CHANNEL (32ksps)
DEDICATED PHYSICAL CHANNEL (64ksps)
DEDICATED PHYSICAL CHANNEL (128ksps)
DEDICATED PHYSICAL CHANNEL (256ksps)
DEDICATED PHYSICAL CHANNEL (512ksps)
DEDICATED PHYSICAL CHANNEL (1024ksps)
BCCH1
BCCH2
PCH
FACH-L
FACH-S
RACH-L
RACH-S
SDCCH
DTCH
ACCH
UPCH

FIG.8

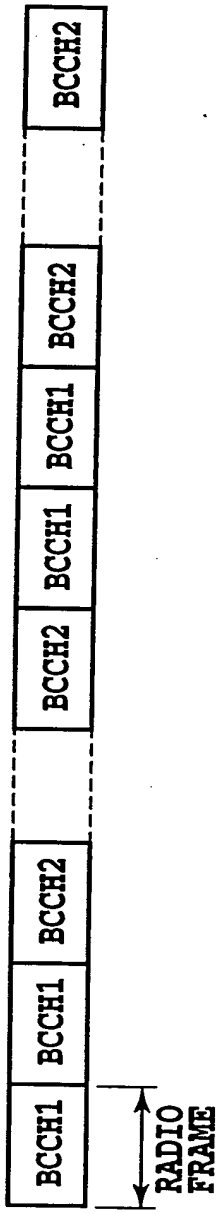

BCCH2
BCCH2
BCCH1
BCCH1
BCCH2
BCCH2
BCCH1
BCCH2
RADIO FRAME

FIG.9

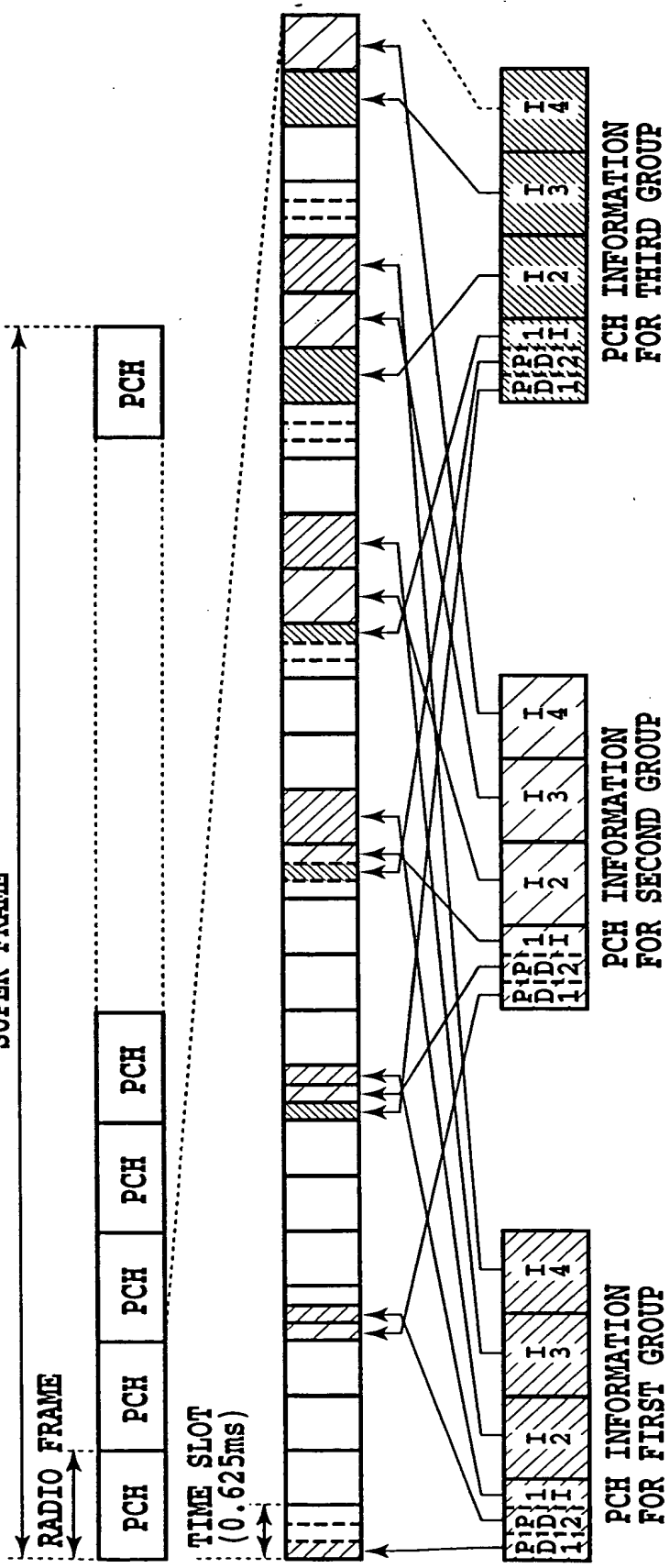

SUPER FRAME
RADIO FRAME
PCH
PCH
PCH
PCH
PCH
TIME SLOT
(0.625ms)
P-ICH
D-ICH
I1
I2
I3
I4
PCH INFORMATION
FOR FIRST GROUP
PCH INFORMATION
FOR SECOND GROUP
PCH INFORMATION
FOR THIRD GROUP

FIG.10

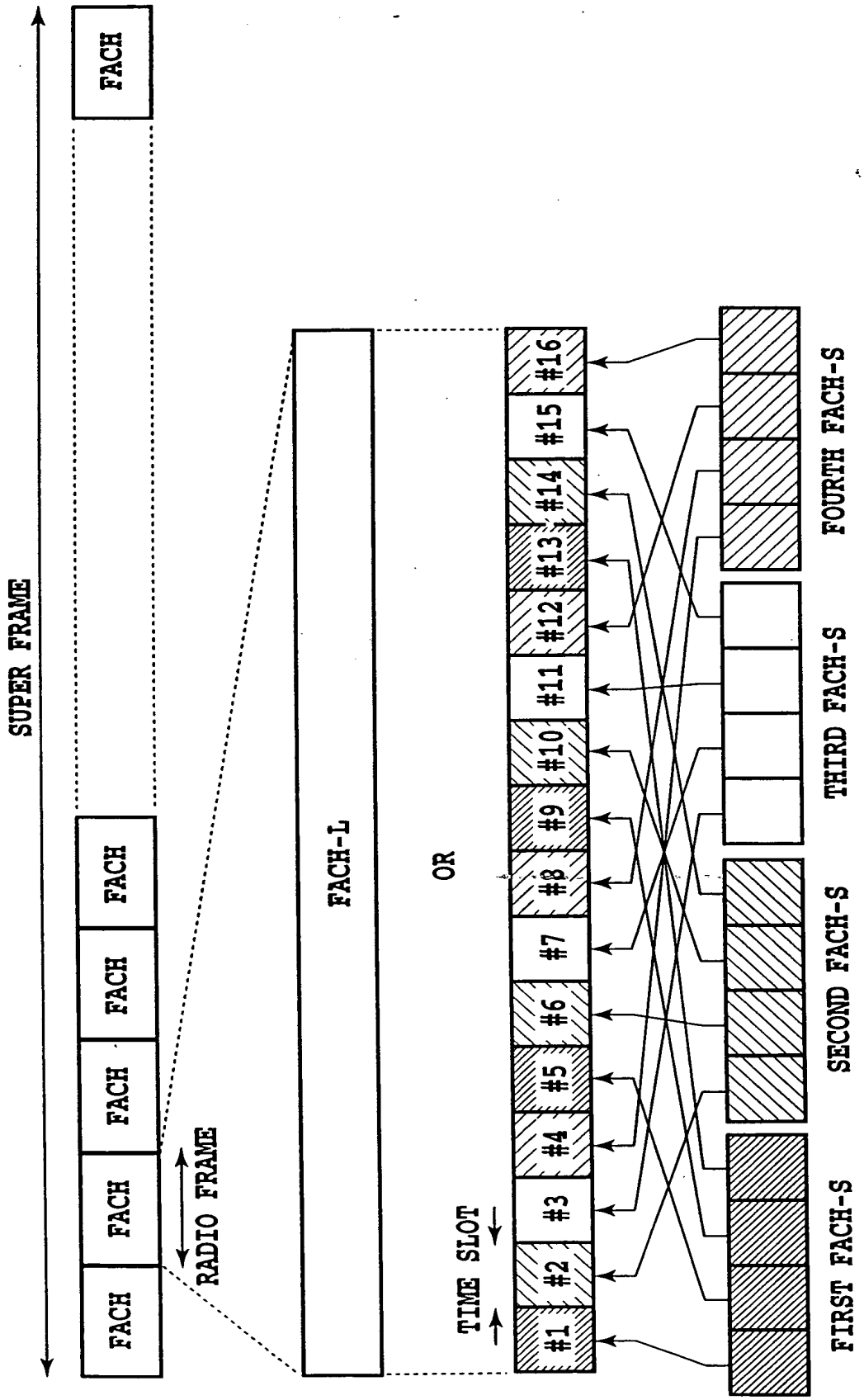

SUPER FRAME
FACH
FACH
FACH
FACH
FACH
RADIO FRAME
FACH-L
OR
TIME SLOT
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
#11
#12
#13
#14
#15
#16
FIRST FACH-S
SECOND FACH-S
THIRD FACH-S
FOURTH FACH-S

FIG.11

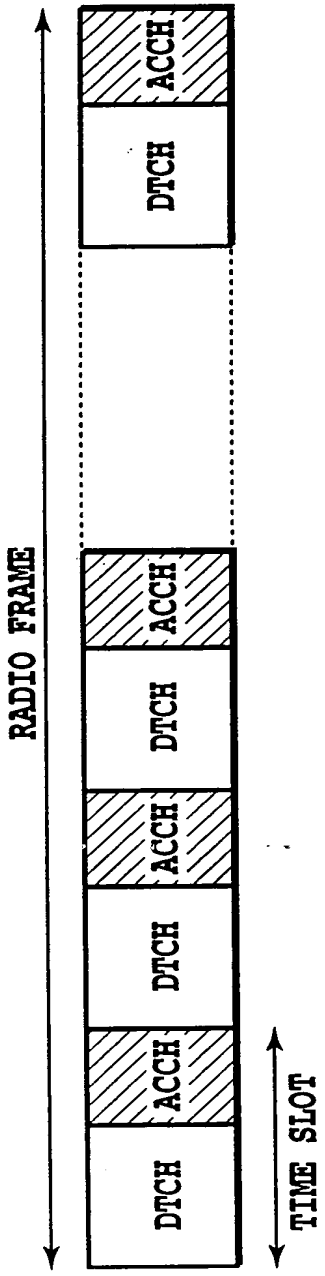

RADIO FRAME
DTCH
ACCH
DTCH
ACCH
DTCH
ACCH
DTCH
ACCH
DTCH
TIME SLOT

FIG.12

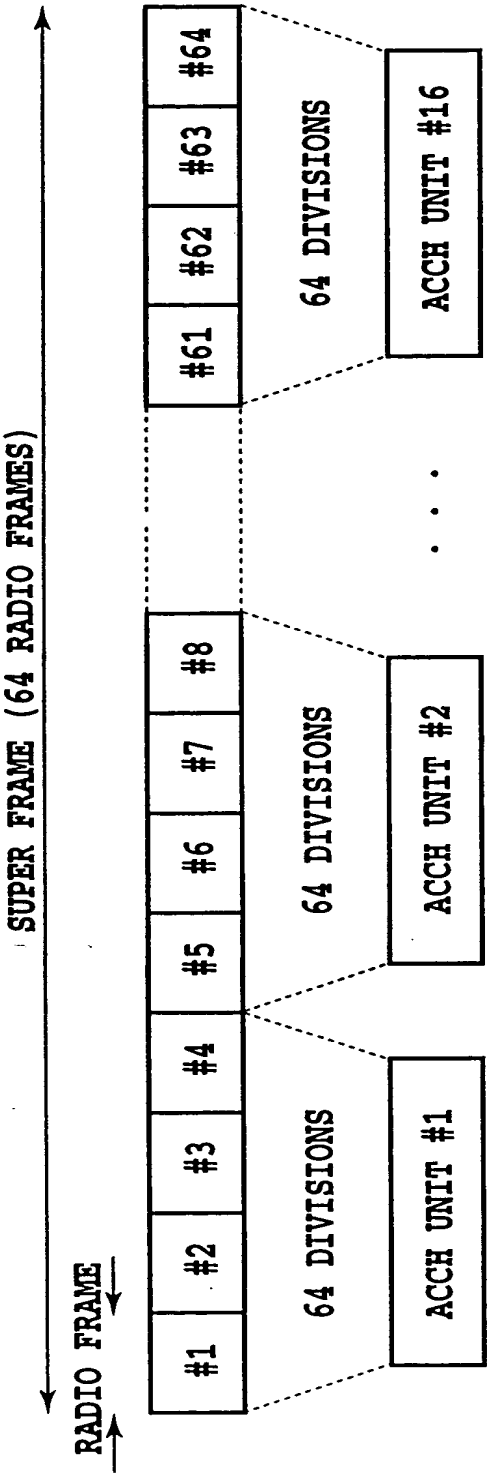

SUPER FRAME (64 RADIO FRAMES)
RADIO FRAME
#1
#2
#3
#4
#5
#6
#7
#8
#61
#62
#63
#64
64 DIVISIONS
64 DIVISIONS
64 DIVISIONS
ACCH UNIT #1
ACCH UNIT #2
ACCH UNIT #16
MAPPING INTO 32 OR 64ksps DEDICATED PHYSICAL CHANNEL

FIG.13A

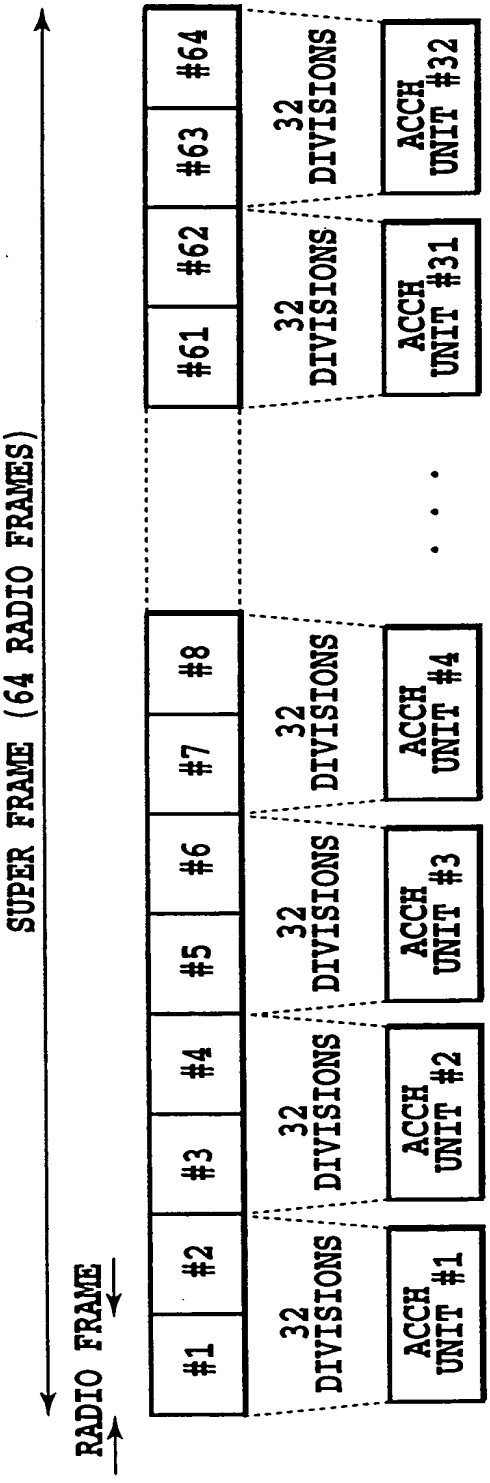

SUPER FRAME (64 RADIO FRAMES)
RADIO FRAME
#1
#2
#3
#4
#5
#6
#7
#8
#61
#62
#63
#64
32 DIVISIONS
ACCH UNIT #1
ACCH UNIT #2
ACCH UNIT #3
ACCH UNIT #4
ACCH UNIT #31
ACCH UNIT #32
MAPPING INTO 128ksps DEDICATED PHYSICAL CHANNEL

FIG.13B

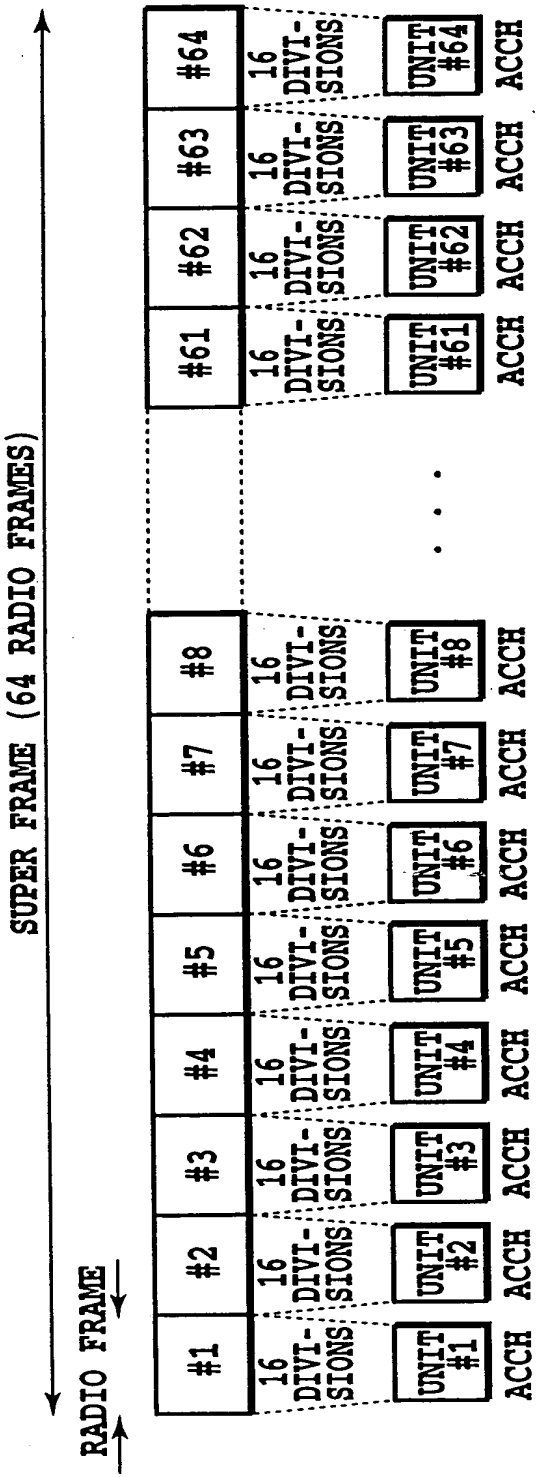

SUPER FRAME (64 RADIO FRAMES)
RADIO FRAME
#1
#2
#3
#4
#5
#6
#7
#8
#61
#62
#63
#64
16 DIVI-SIONS
UNIT #1
UNIT #2
UNIT #3
UNIT #4
UNIT #5
UNIT #6
UNIT #7
UNIT #8
UNIT #61
UNIT #62
UNIT #63
UNIT #64
ACCH
MAPPING INTO 256ksps DEDICATED PHYSICAL CHANNEL

FIG.13C

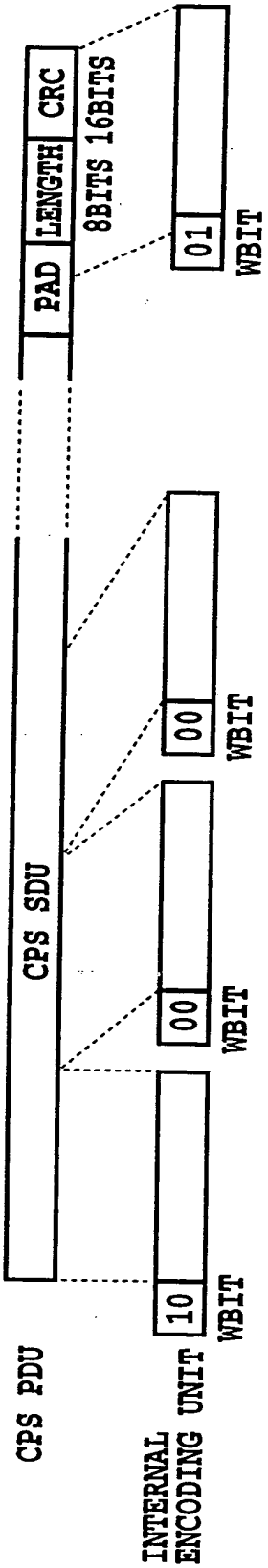

CPS PDU
CPS SDU
PAD
LENGTH
CRC
8BITS 16BITS
INTERNAL ENCODING UNIT
10
00
00
01
WBIT
WBIT
WBIT
WBIT

FIG.14

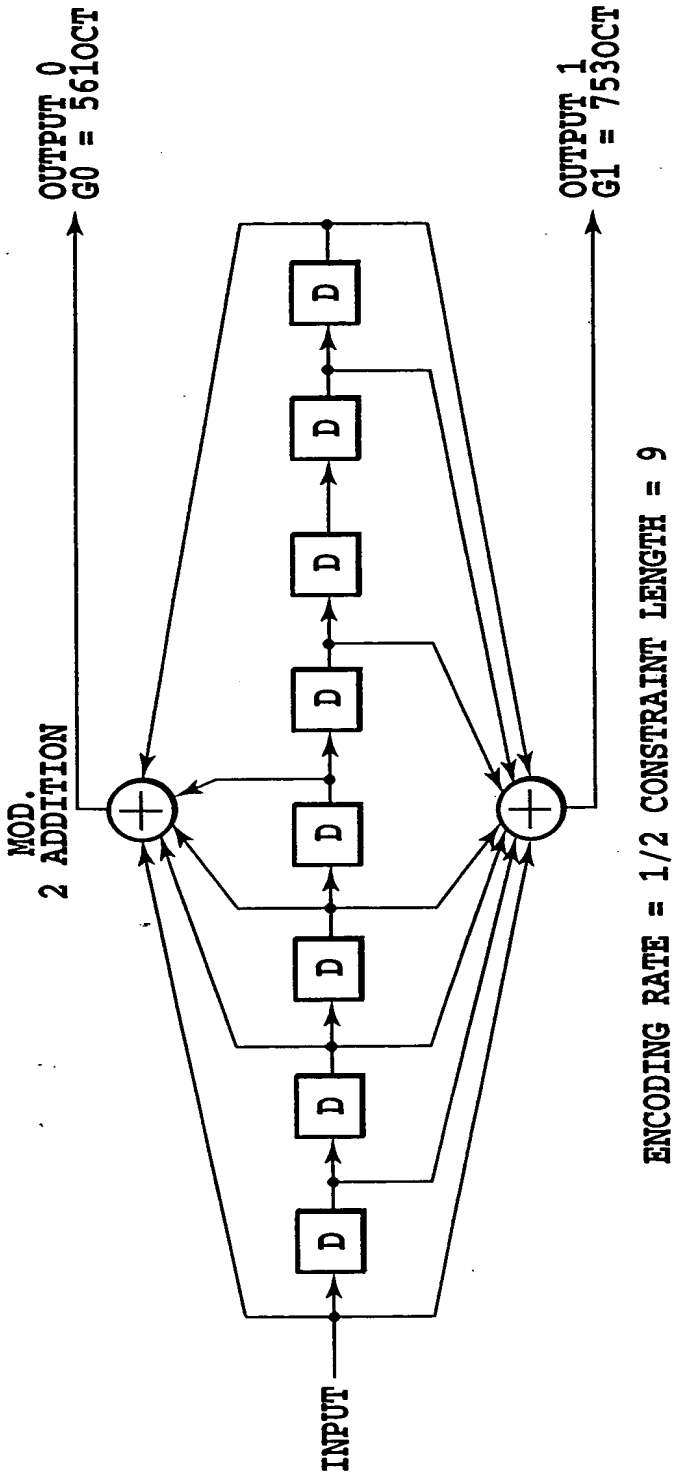

OUTPUT 0
G0 = 561OCT
OUTPUT 1
G1 = 753OCT
MOD.
2 ADDITION
D
INPUT
ENCODING RATE = 1/2 CONSTRAINT LENGTH = 9

FIG.15A

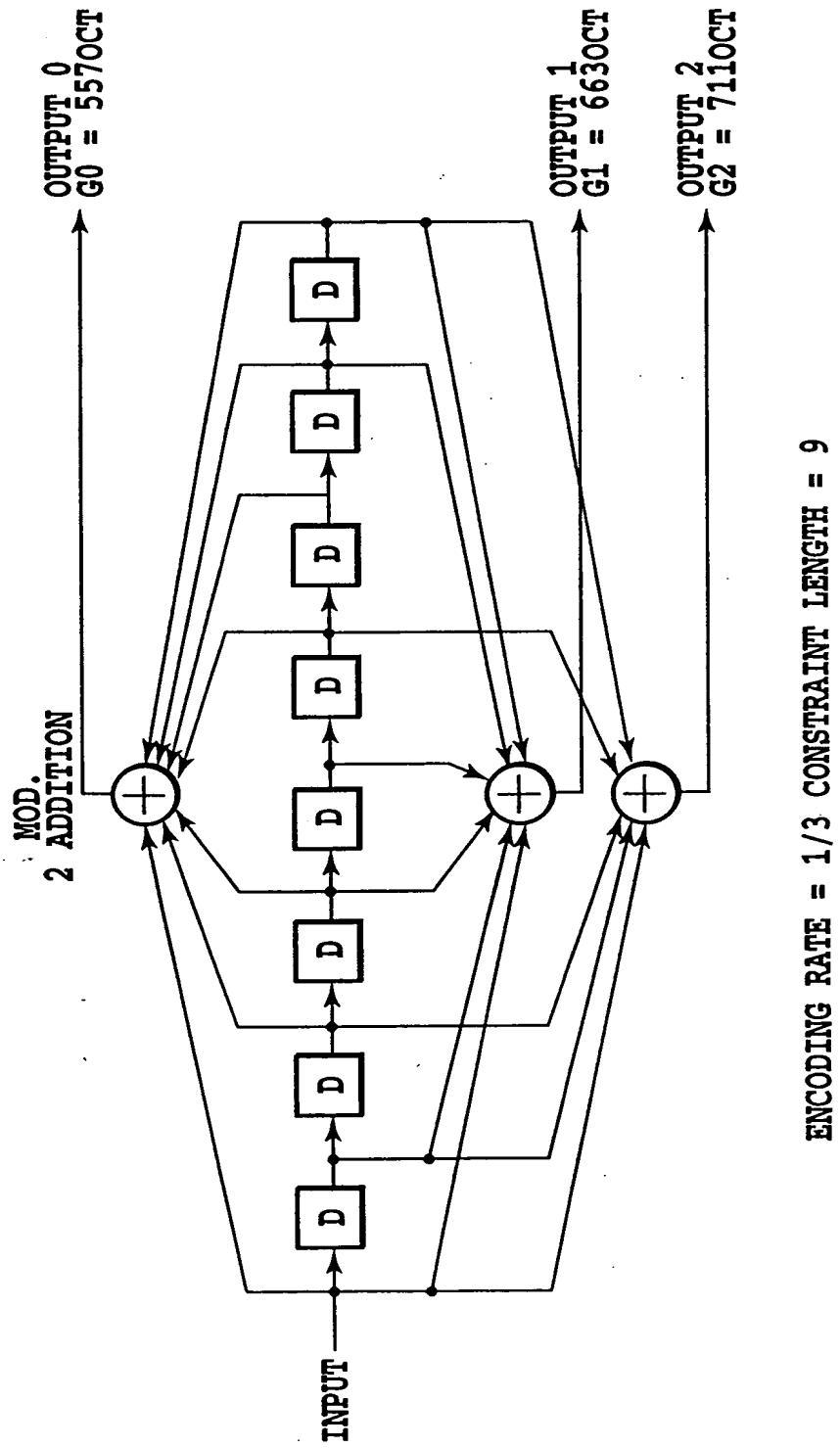

OUTPUT 0
G0 = 557OCT
OUTPUT 1
G1 = 663OCT
OUTPUT 2
G2 = 711OCT
MOD.
2 ADDITION
D
INPUT
ENCODING RATE = 1/3 CONSTRAINT LENGTH = 9

FIG.15B

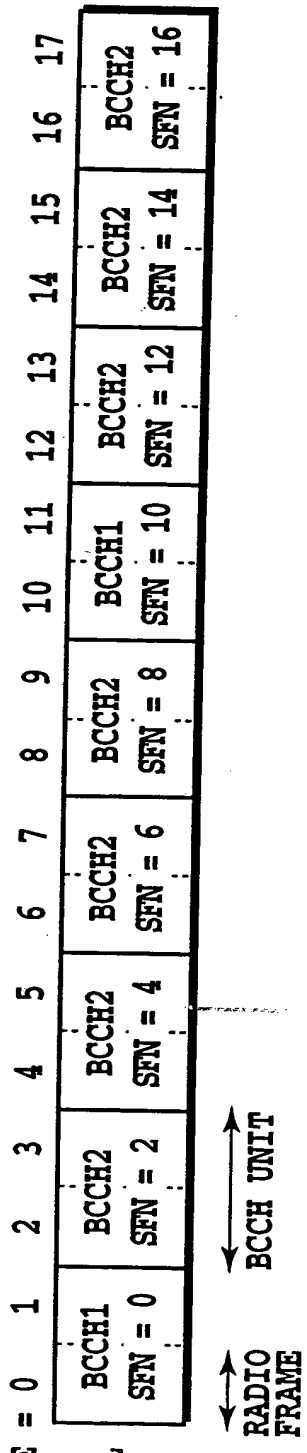

SFN VALUE = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
PERCH CHANNEL
BCCH1 SFN = 0
BCCH2 SFN = 2
BCCH2 SFN = 4
BCCH2 SFN = 6
BCCH2 SFN = 8
BCCH1 SFN = 10
BCCH2 SFN = 12
BCCH2 SFN = 14
BCCH2 SFN = 16
RADIO FRAME
BCCH UNIT

FIG.16

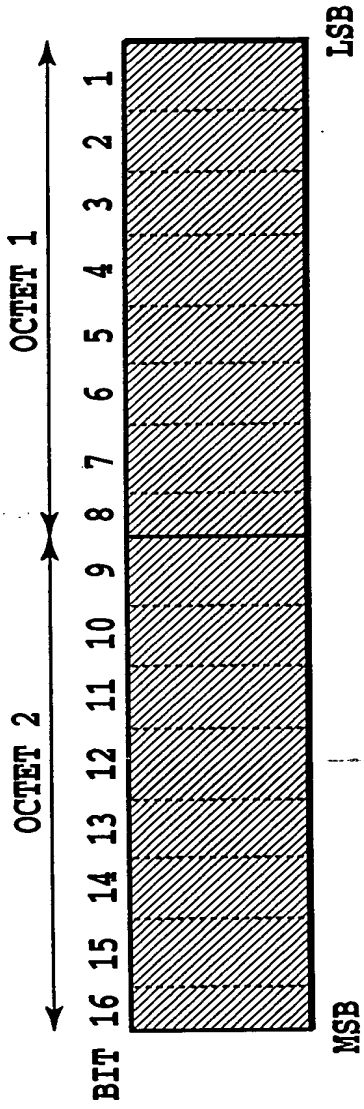


FIG.17

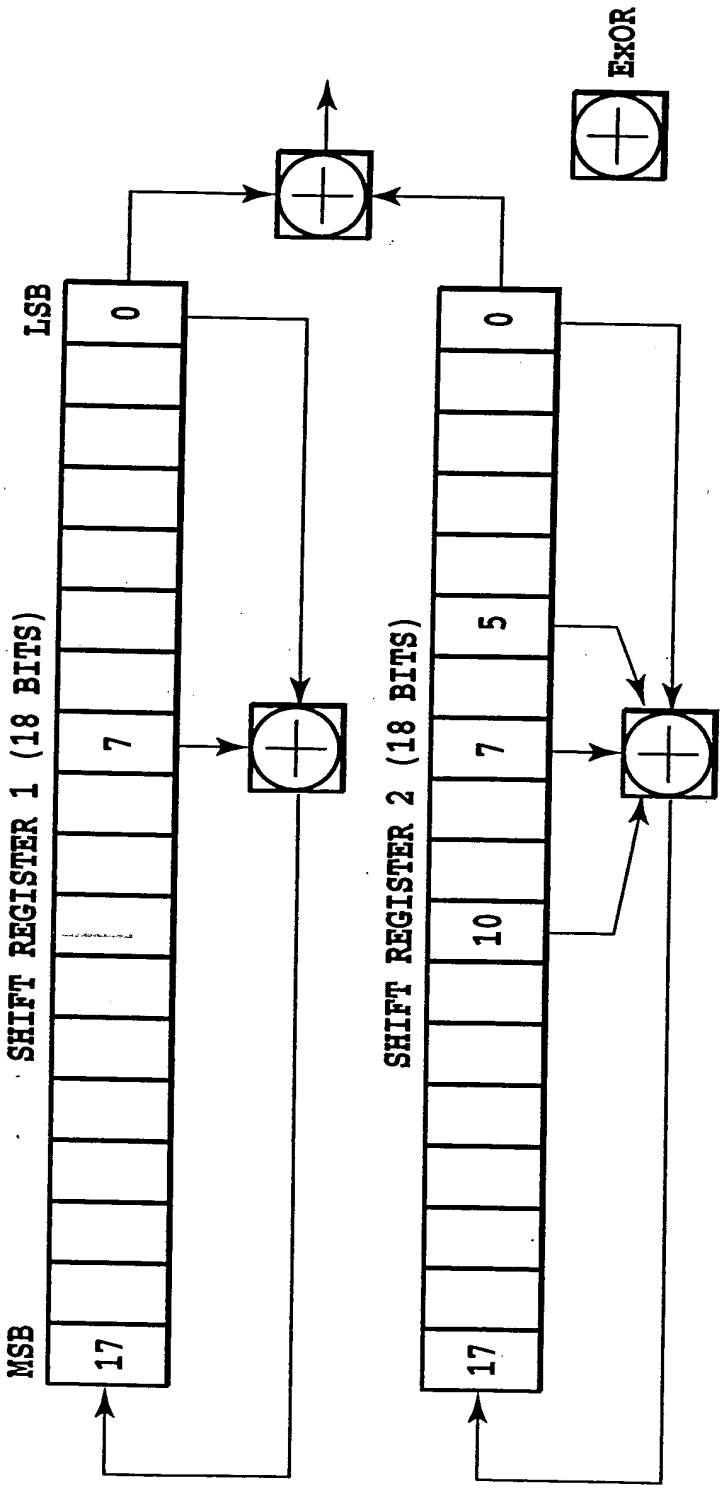

ExOR
LSB
0
SHIFT REGISTER 1 (18 BITS)
7
MSB
17
0
SHIFT REGISTER 2 (18 BITS)
5
7
10
17

FIG.18

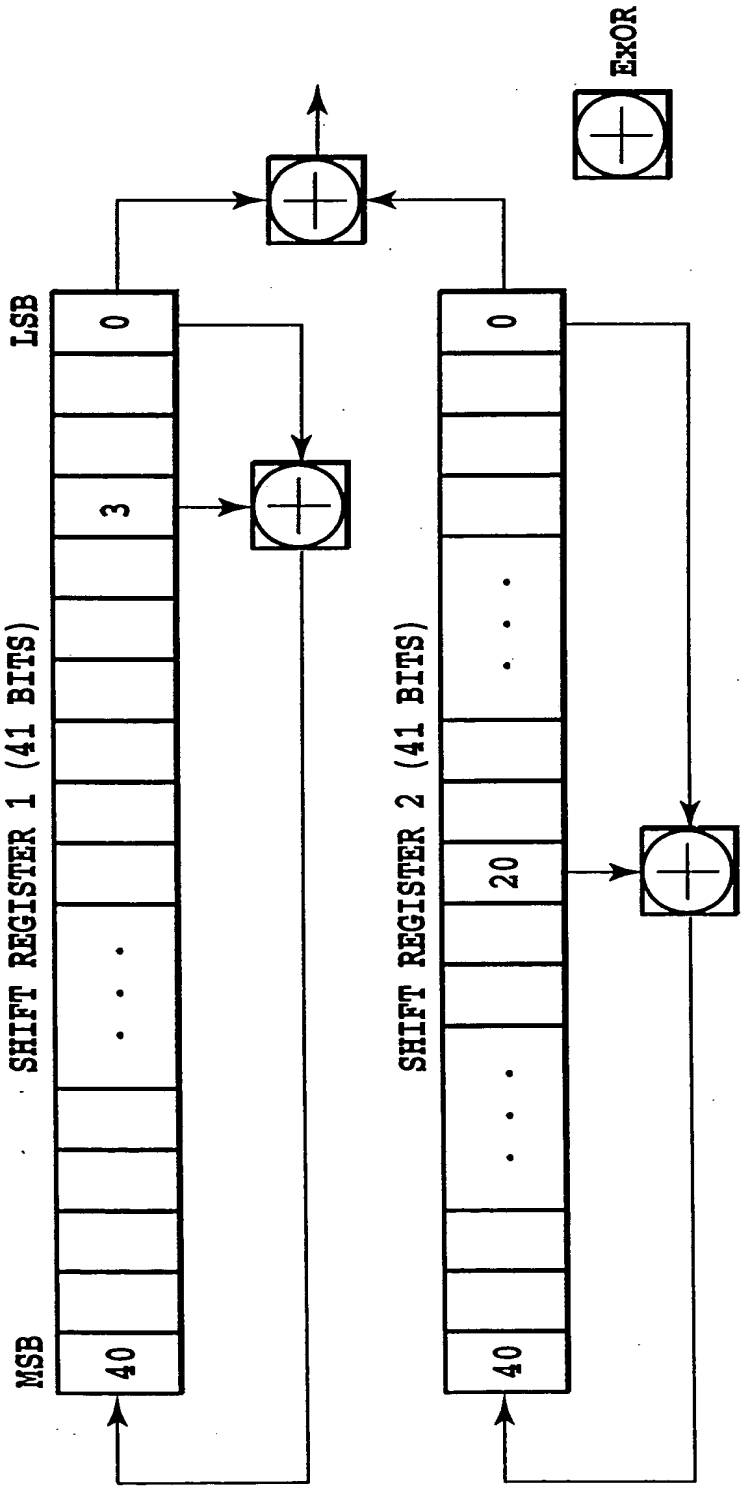

ExOR
LSB
0
3
SHIFT REGISTER 1 (41 BITS)
MSB
40
0
20
SHIFT REGISTER 2 (41 BITS)
40

FIG.19

$$C_0(0)=1$$

$$\begin{bmatrix} C_1(0) \\ C_1(1) \end{bmatrix} = \begin{bmatrix} C_0(0) & C_0(0) \\ C_0(0) & \overline{C_0(0)} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & 0 \end{bmatrix}$$

$$\begin{bmatrix} C_2(0) \\ C_2(1) \\ C_2(2) \\ C_2(3) \end{bmatrix} = \begin{bmatrix} C_1(0) & C_1(0) \\ C_1(0) & \overline{C_1(0)} \\ C_1(1) & C_1(1) \\ C_1(1) & \overline{C_1(1)} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix}$$

$$\vdots$$

$$\begin{bmatrix} C_{n+1}(0) \\ C_{n+1}(1) \\ C_{n+1}(2) \\ C_{n+1}(3) \\ \vdots \\ C_{n+1}(2^{n+1}-2) \\ C_{n+1}(2^{n+1}-1) \end{bmatrix} = \begin{bmatrix} C_n(0) & C_n(0) \\ C_n(0) & \overline{C_n(0)} \\ C_n(1) & C_n(1) \\ C_n(1) & \overline{C_n(1)} \\ \vdots & \vdots \\ C_n(2^n-1) & C_n(2^n-1) \\ C_n(2^n-1) & \overline{C_n(2^n-1)} \end{bmatrix}$$

FIG.20

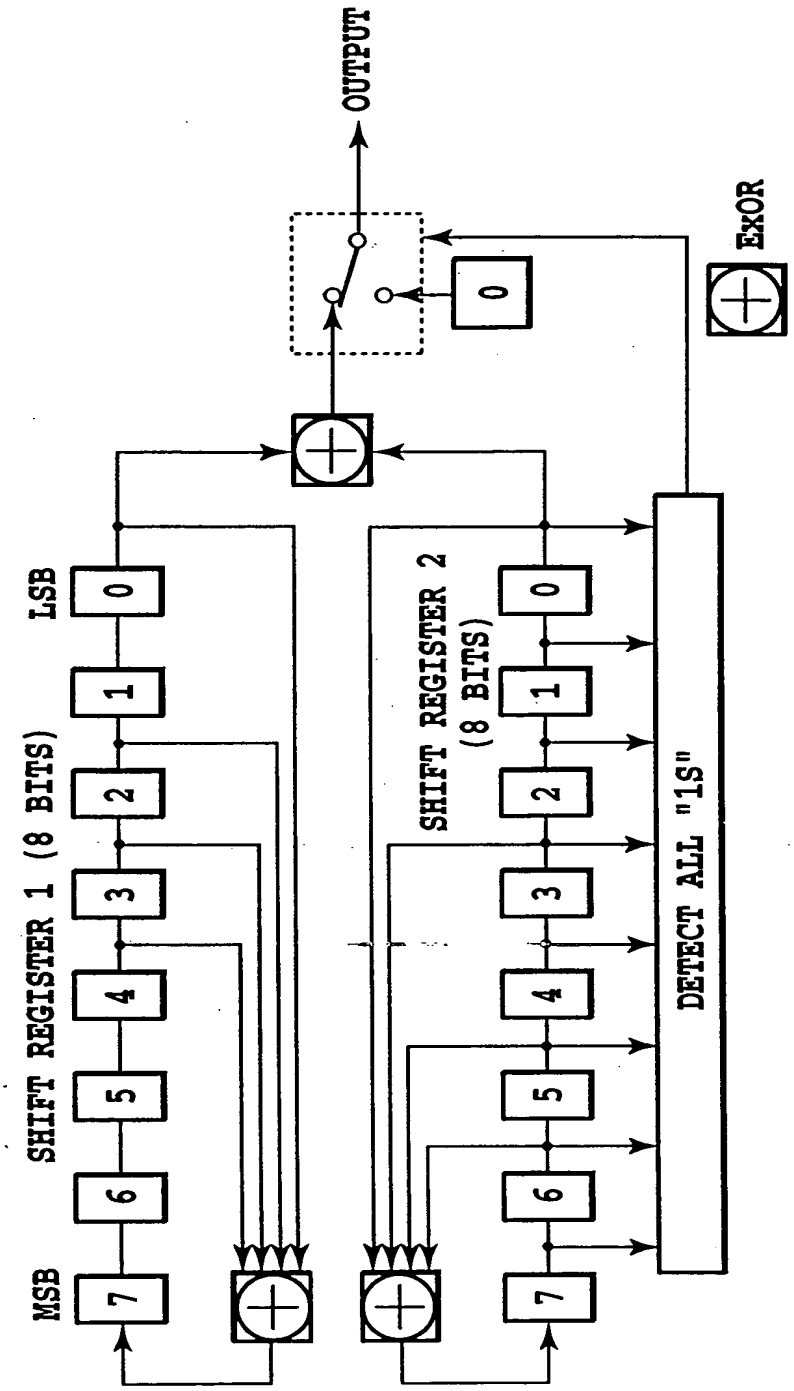

OUTPUT
EXOR
0
LSB
MSB
SHIFT REGISTER 1 (8 BITS)
SHIFT REGISTER 2
(8 BITS)
DETECT ALL "1S"
0
1
2
3
4
5
6
7

FIG.21

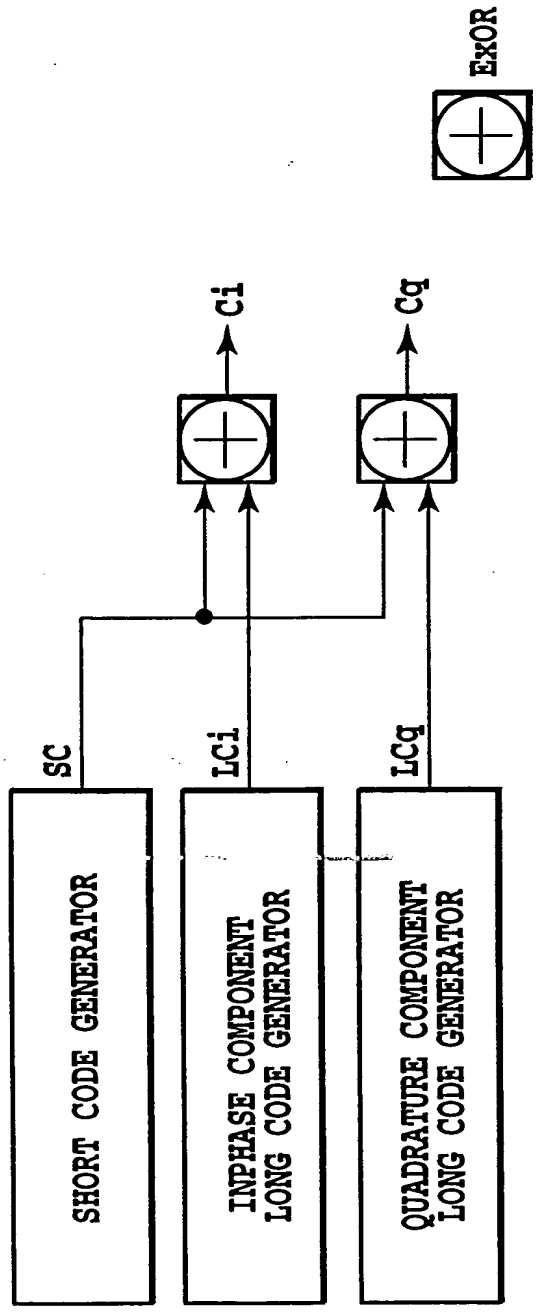

ExOR
Ci
Cq
SC
LCi
LCq
SHORT CODE GENERATOR
INPHASE COMPONENT LONG CODE GENERATOR
QUADRATURE COMPONENT LONG CODE GENERATOR

FIG.22

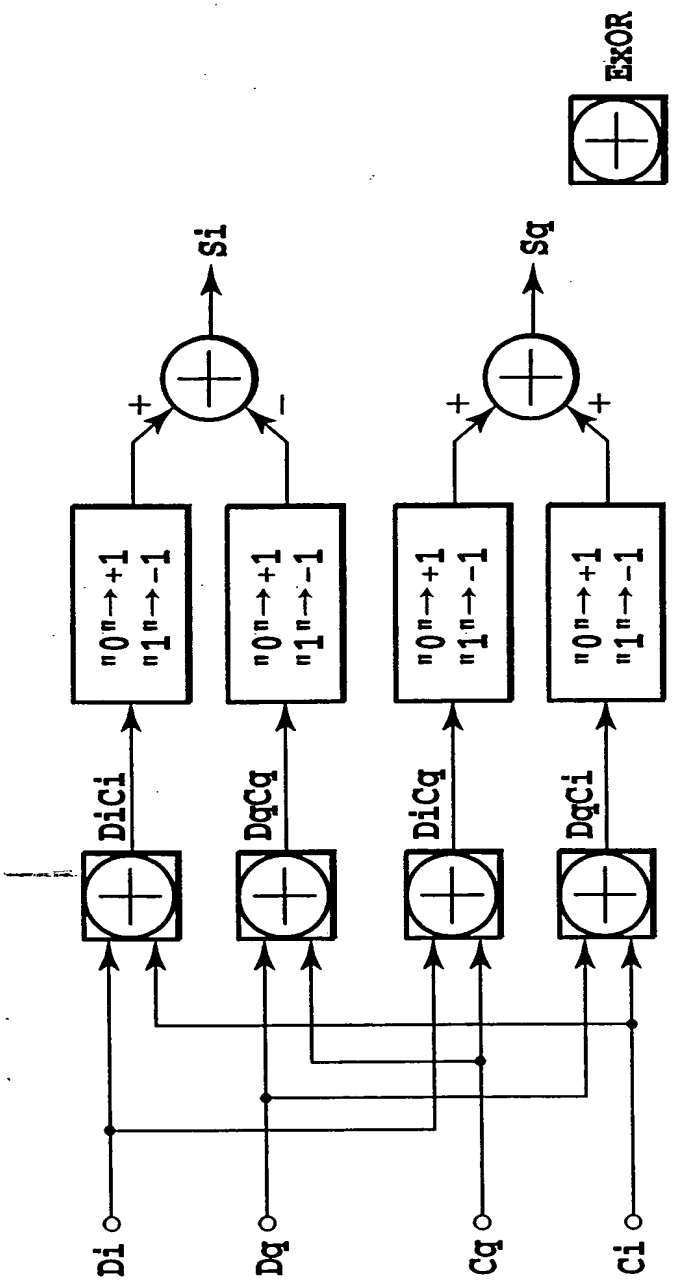


FIG.23

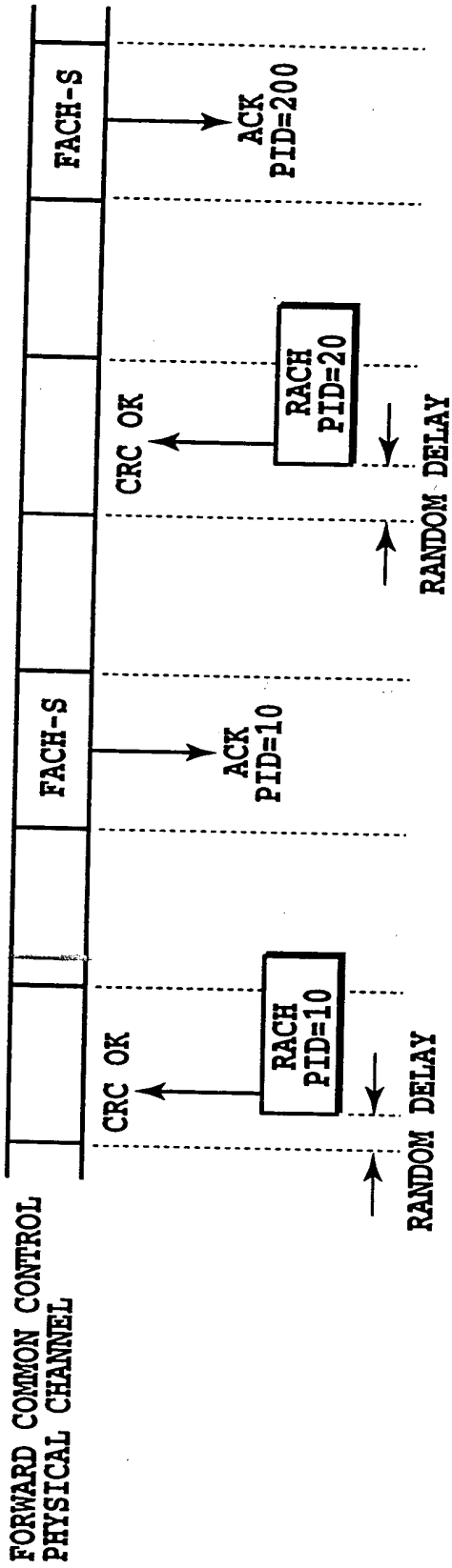

FORWARD COMMON CONTROL PHYSICAL CHANNEL
FACH-S
ACK PID=200
RACH PID=20
CRC OK
RANDOM DELAY
FACH-S
ACK PID=10
RACH PID=10
CRC OK
RANDOM DELAY

FIG.24

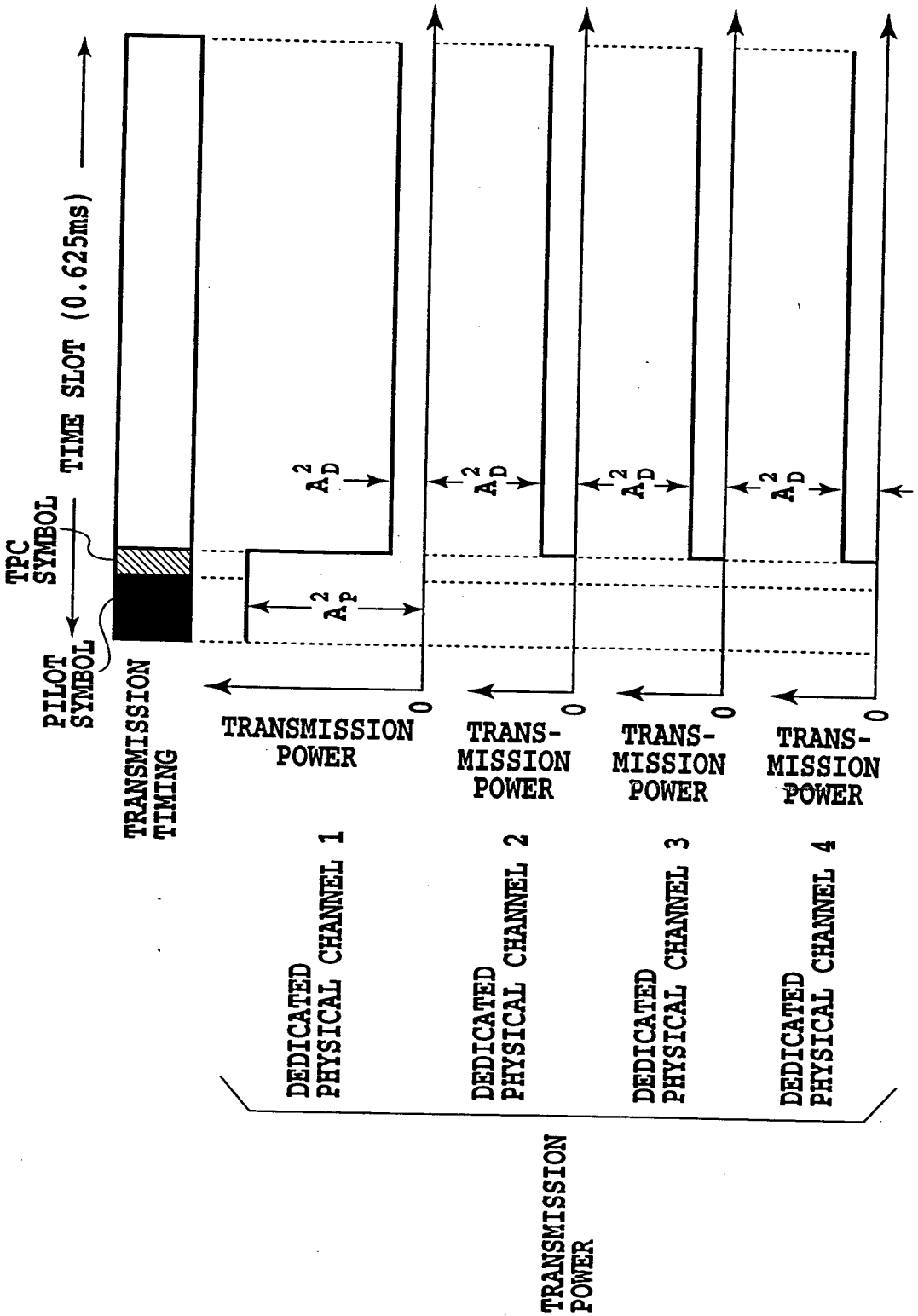

TIME SLOT (0.625ms)
TPC SYMBOL
PILOT SYMBOL
TRANSMISSION TIMING
A_P^2
A_D^2
TRANSMISSION POWER
TRANS-MISSION POWER
TRANS-MISSION POWER
TRANS-MISSION POWER
0
DEDICATED PHYSICAL CHANNEL 1
DEDICATED PHYSICAL CHANNEL 2
DEDICATED PHYSICAL CHANNEL 3
DEDICATED PHYSICAL CHANNEL 4
TRANSMISSION POWER

FIG.25

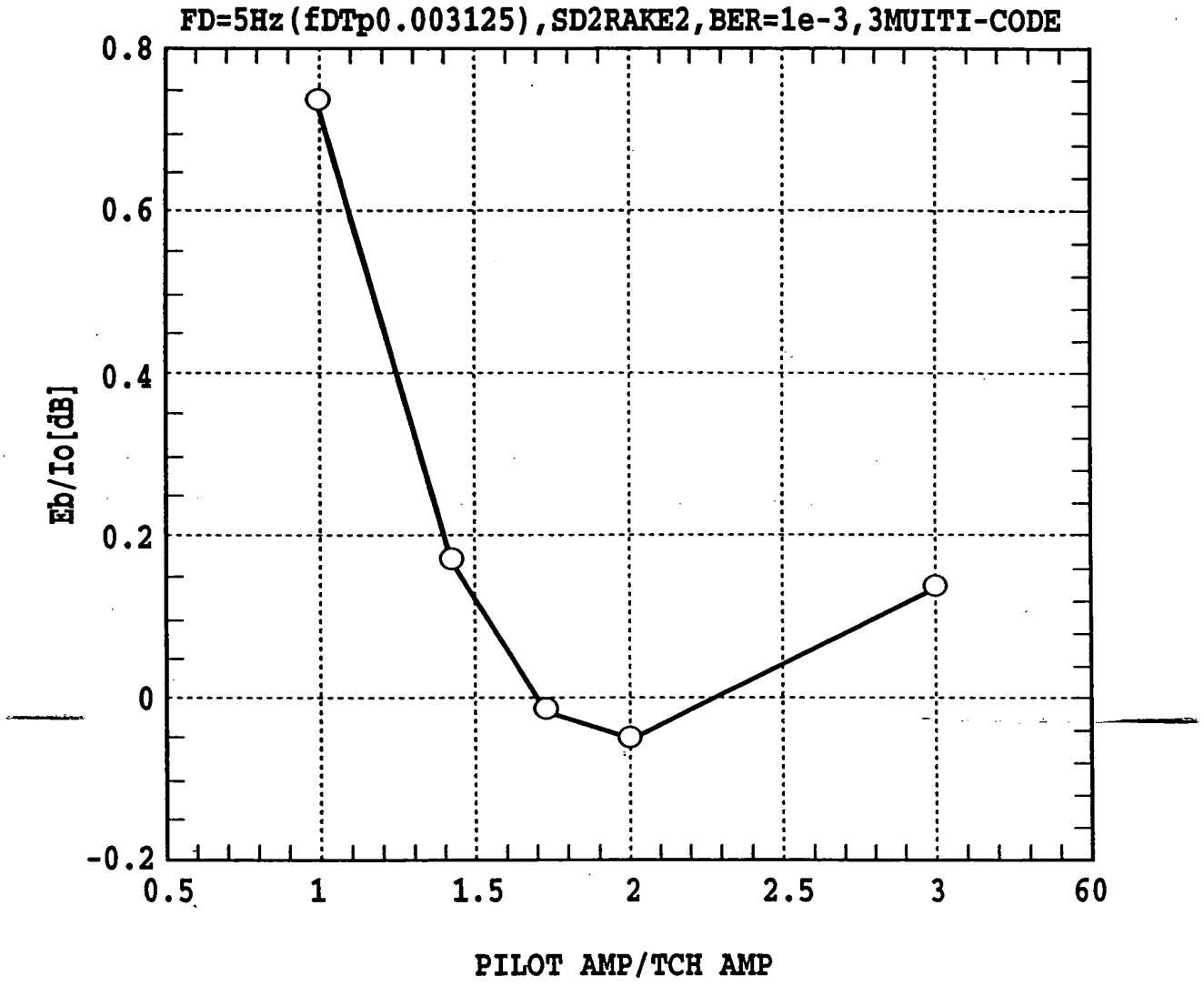

FD=5Hz(fDTp0.003125),SD2RAKE2,BER=1e-3,3MUITI-CODE
0.8
0.6
0.4
0.2
0
-0.2
Eb/Io[dB]
0.5
1
1.5
2
2.5
3
60
PILOT AMP/TCH AMP

FIG.26

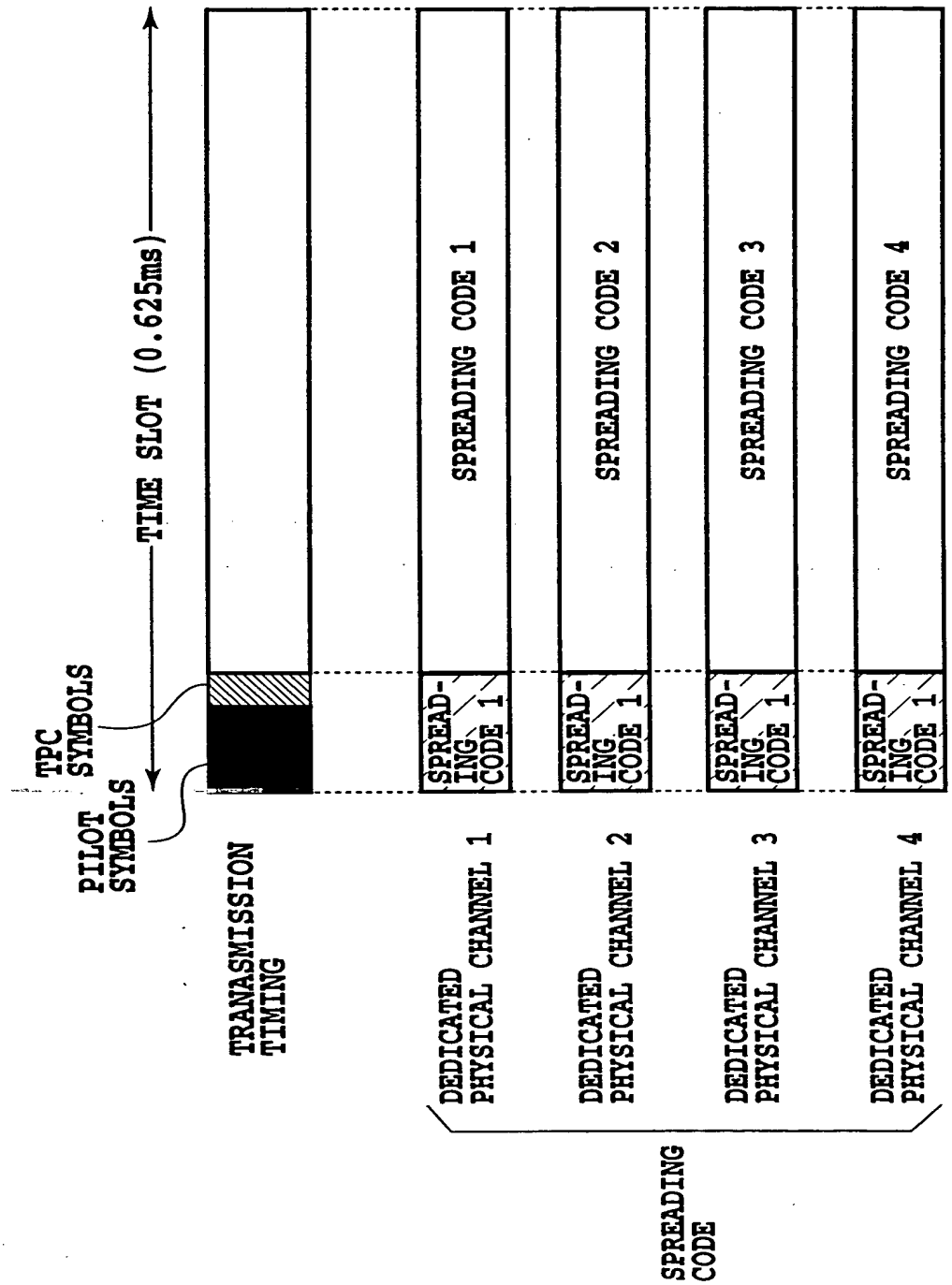
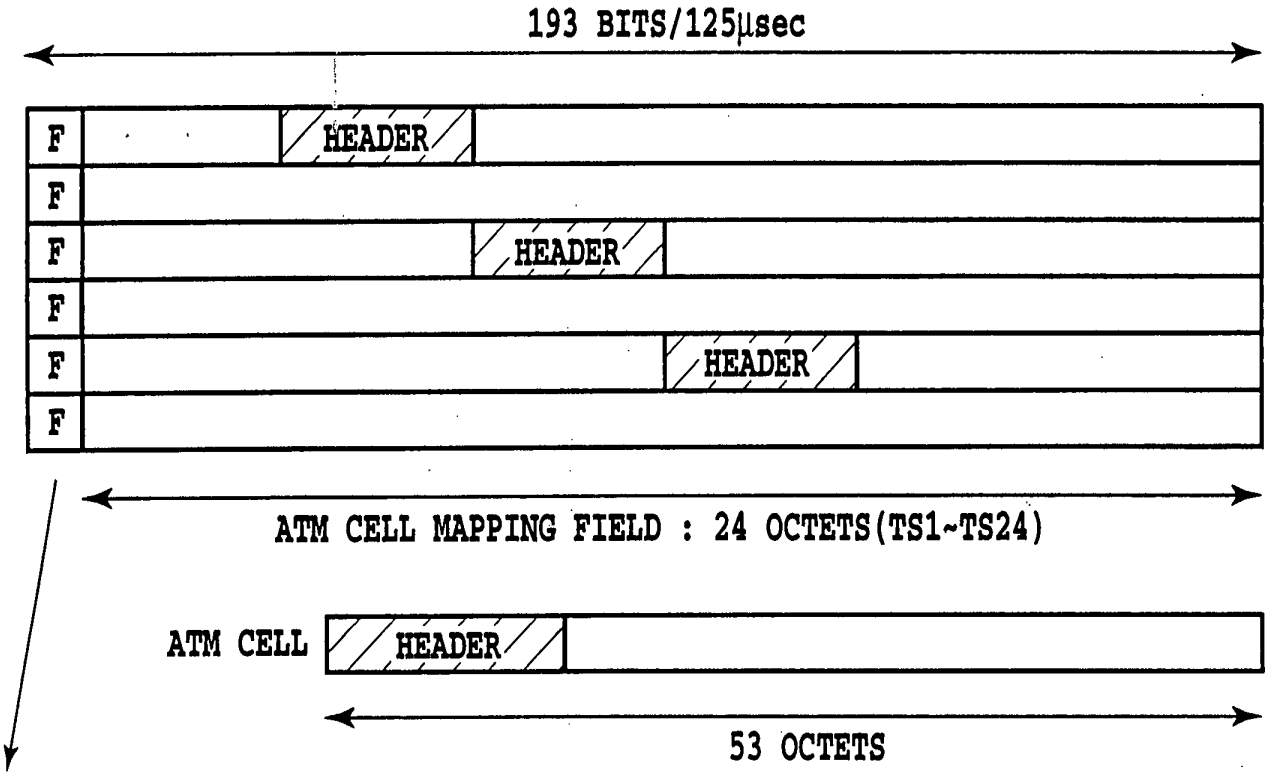

TIME SLOT (0.625ms)
TPC SYMBOLS
PILOT SYMBOLS
TRANASMISSION TIMING
SPREADING CODE 1
SPREADING CODE 2
SPREADING CODE 3
SPREADING CODE 4
SPREAD-ING CODE 1
SPREAD-ING CODE 1
SPREAD-ING CODE 1
SPREAD-ING CODE 1
DEDICATED PHYSICAL CHANNEL 1
DEDICATED PHYSICAL CHANNEL 2
DEDICATED PHYSICAL CHANNEL 3
DEDICATED PHYSICAL CHANNEL 4
SPREADING CODE

FIG.27

FIG.28A



PROVIDES F3 OAM FUNCTIONS:
-DETECTION OF LOSS FRAME ALIGNMENT
-PERFORMANCE MONITORING(CRC-6)
-TRANSMISSION OF FERF AND LOC
-PERFORMANCE REPORTING

FIG.28B

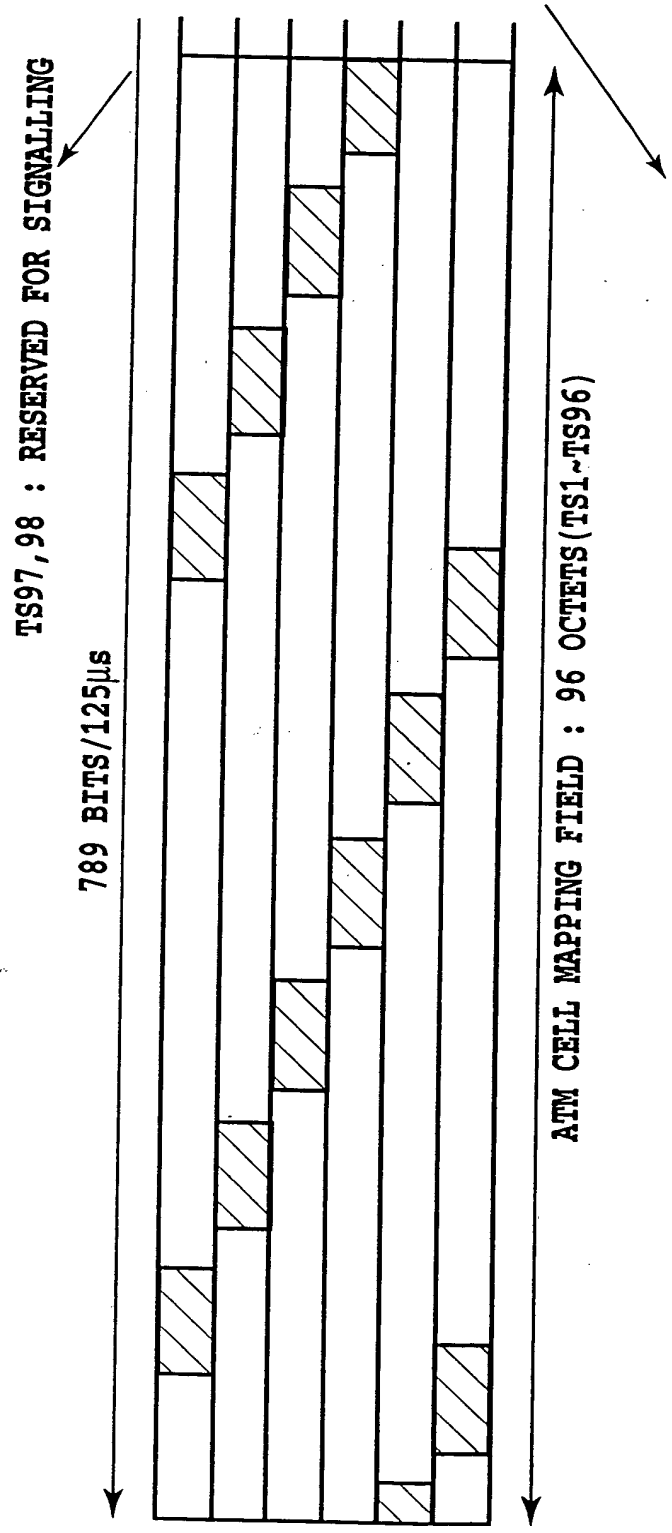


FIG.29A

PROVIDES F3 OAM FUNCTIONS:
-DETECTION OF LOSS FRAME ALIGNMENT
-PERFORMANCE MONITORING(CRC-5)
-TRANSMISSION OF FERF AND LOC
-PERFORMANCE REPORTING

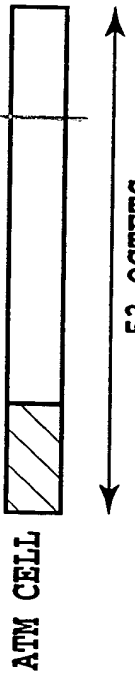
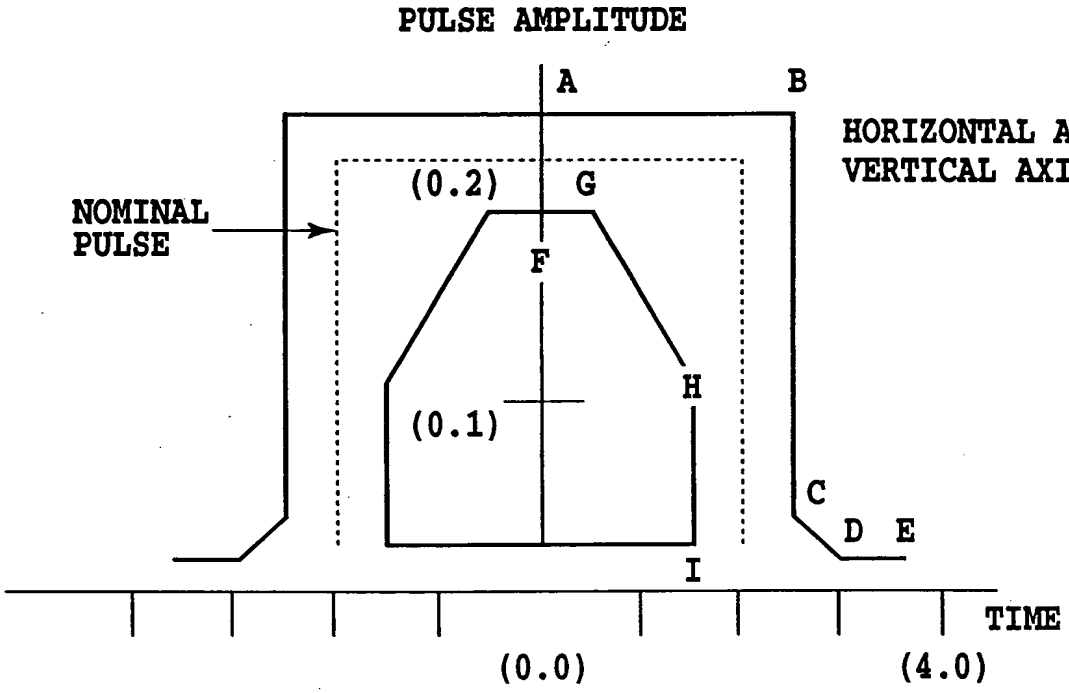


FIG.29B



COORDINATES OF
INTERSECTION POINTS

A : (0, 2.3)	F : (0, 1.7)
B : (2.4, 2.3)	G : (0.4, 1.7)
C : (2.4, 1.0)	H : (1.6, 0.9)
D : (3.2, 0.3)	I : (1.6, 0.3)
E : (4.0, 0.3)	

FIG.30

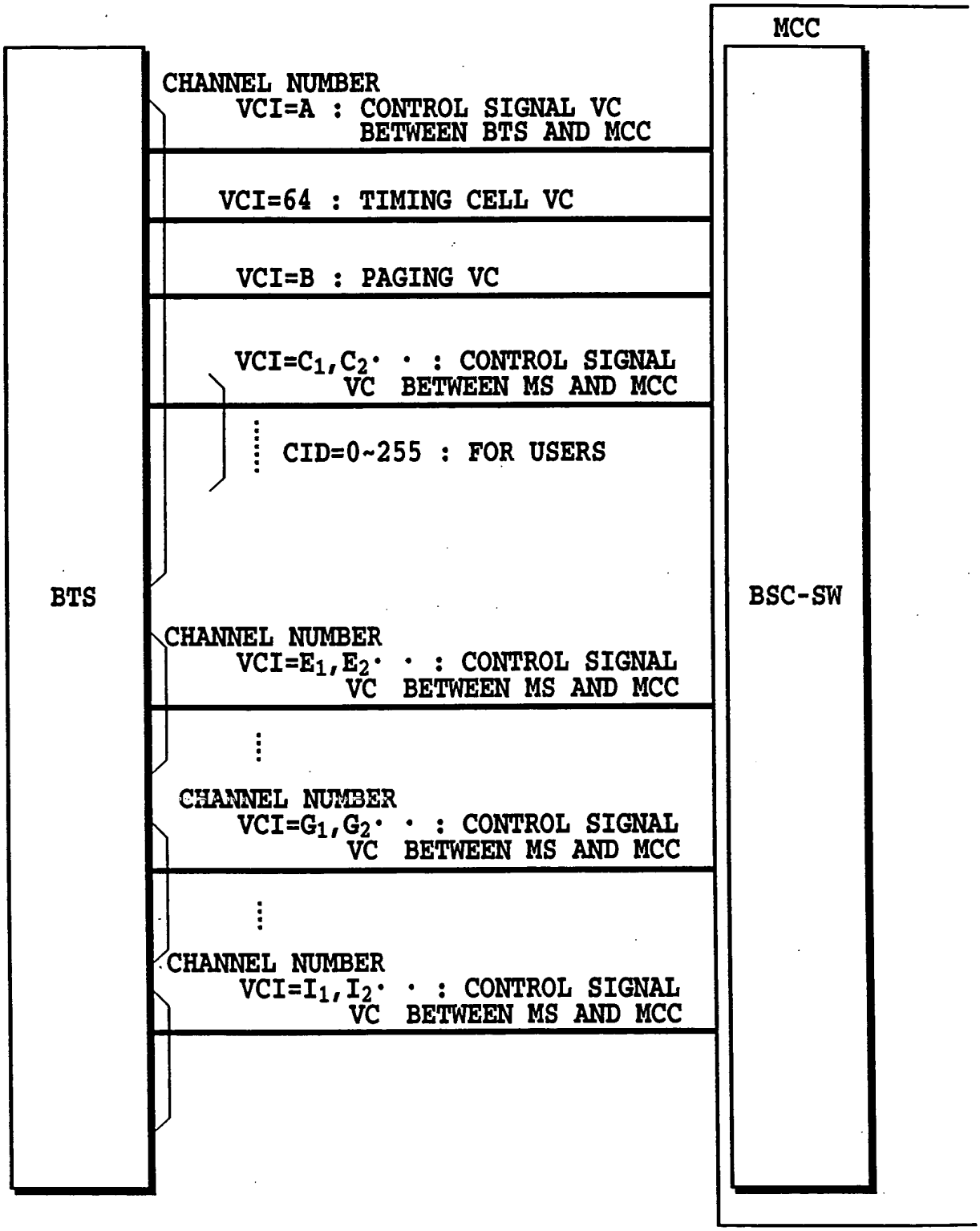

MCC
CHANNEL NUMBER
VCI=A : CONTROL SIGNAL VC
BETWEEN BTS AND MCC
VCI=64 : TIMING CELL VC
VCI=B : PAGING VC
VCI=C1,C2 : CONTROL SIGNAL
VC BETWEEN MS AND MCC
CID=0~255 : FOR USERS
BTS
BSC-SW
CHANNEL NUMBER
VCI=E1,E2 : CONTROL SIGNAL
VC BETWEEN MS AND MCC
CHANNEL NUMBER
VCI=G1,G2 : CONTROL SIGNAL
VC BETWEEN MS AND MCC
CHANNEL NUMBER
VCI=I1,I2 : CONTROL SIGNAL
VC BETWEEN MS AND MCC

FIG.31

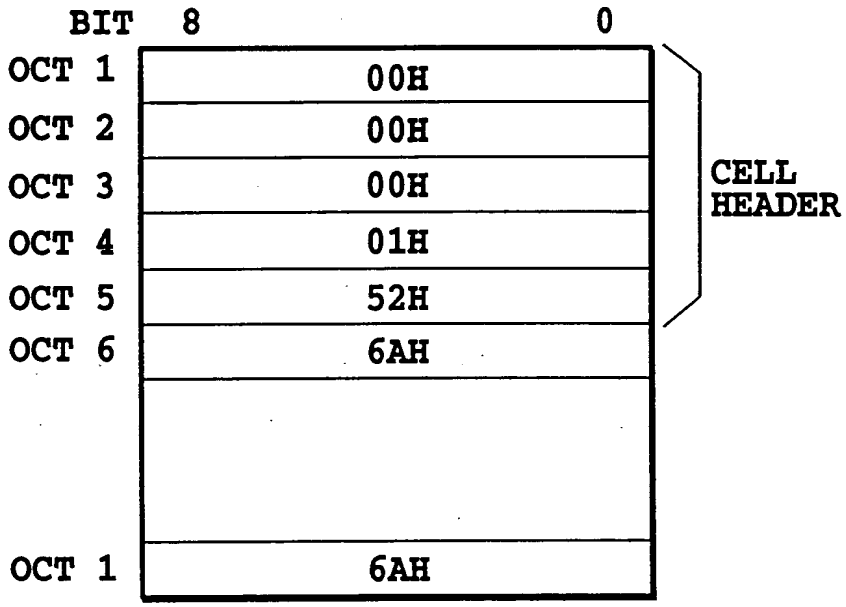

BIT 8
0
OCT 1
00H
OCT 2
00H
OCT 3
00H
OCT 4
01H
OCT 5
52H
OCT 6
6AH
OCT 1
6AH
CELL HEADER

FIG.32

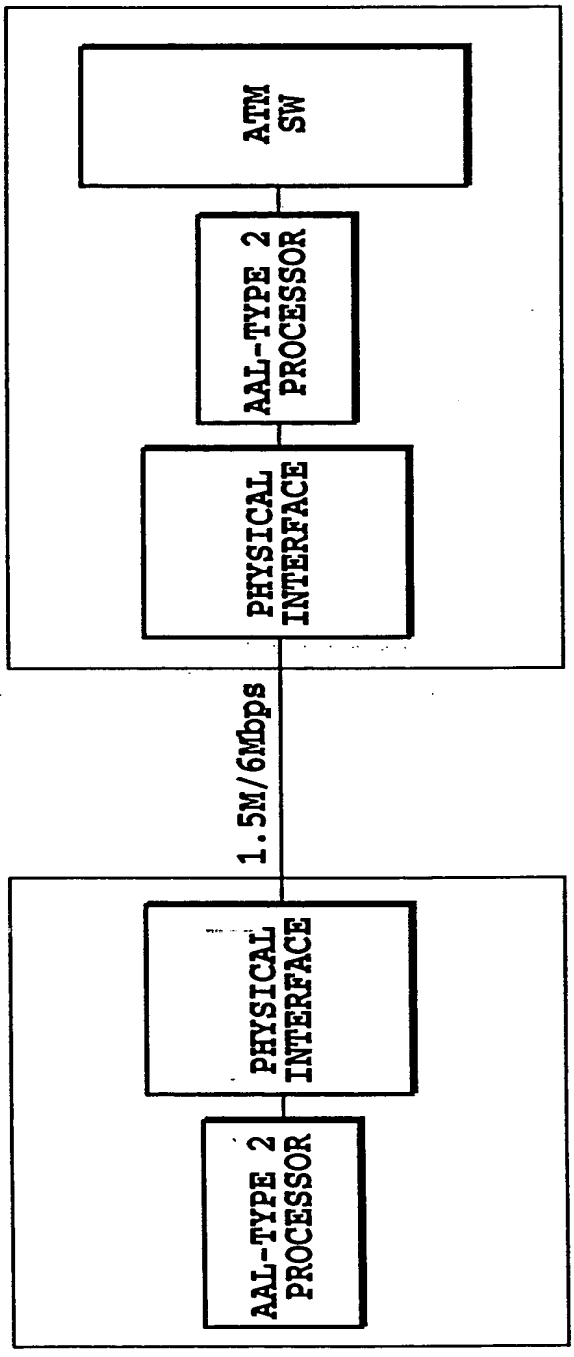


FIG.33A

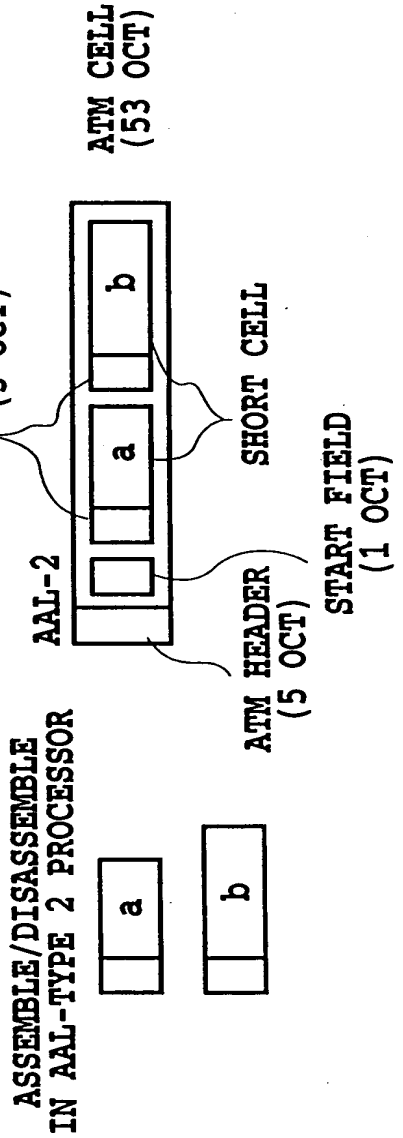


FIG.33B

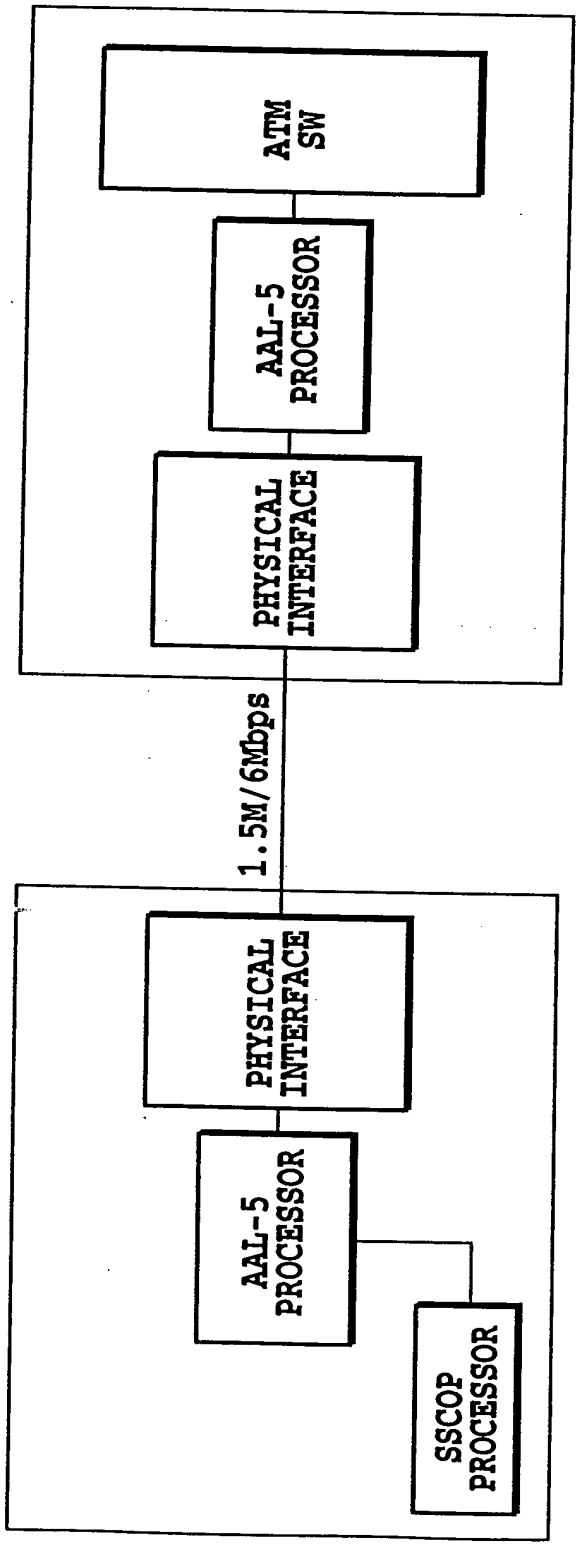
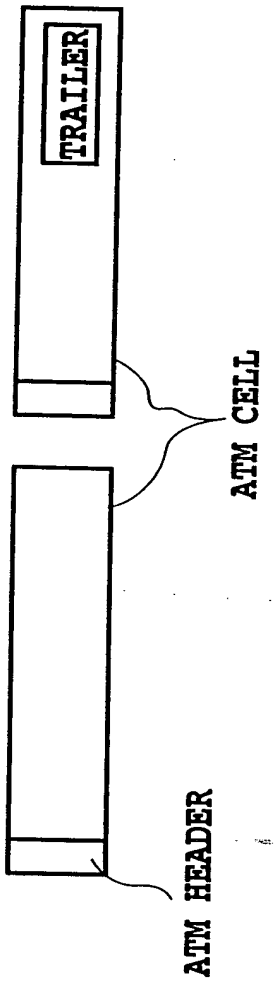
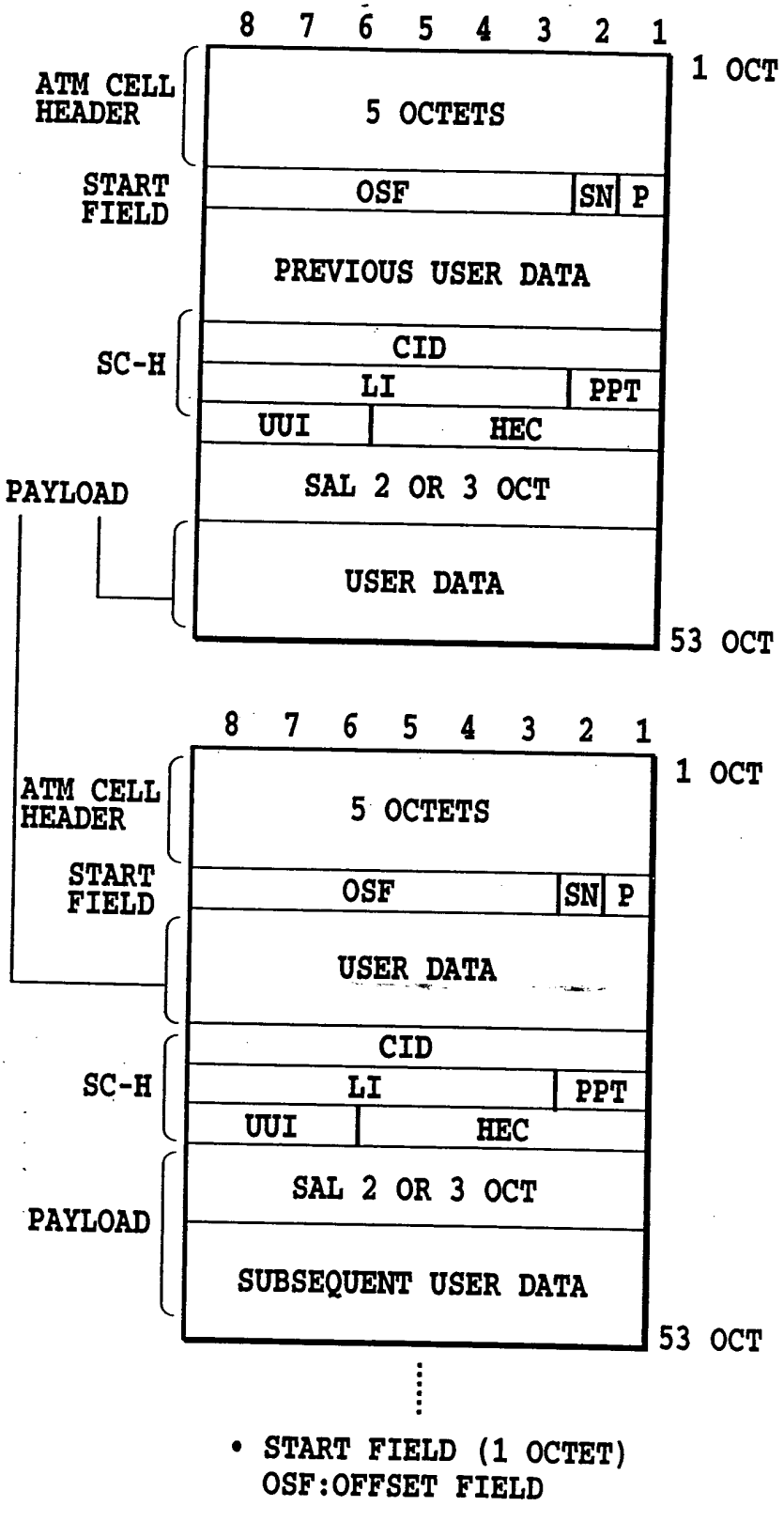


FIG.34A



ASSEMBLE/DISASSEMBLE IN AAL-5 PROCESSOR

FIG.34B



• START FIELD (1 OCTET)
OSF:OFFSET FIELD

FIG.35

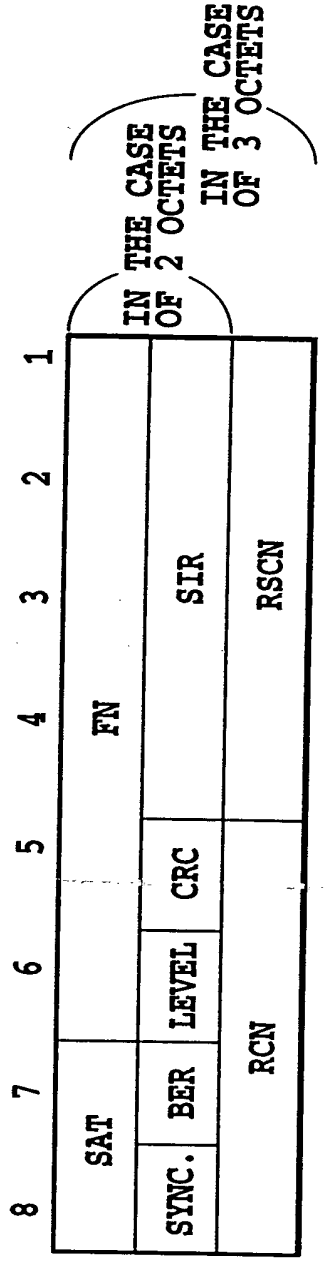

IN THE CASE OF 2 OCTETS
IN THE CASE OF 3 OCTETS
1
2
3
4
5
6
7
8
FN
SIR
RSCN
CRC
LEVEL
BER
SYNC.
SAT
RCN

FIG.36

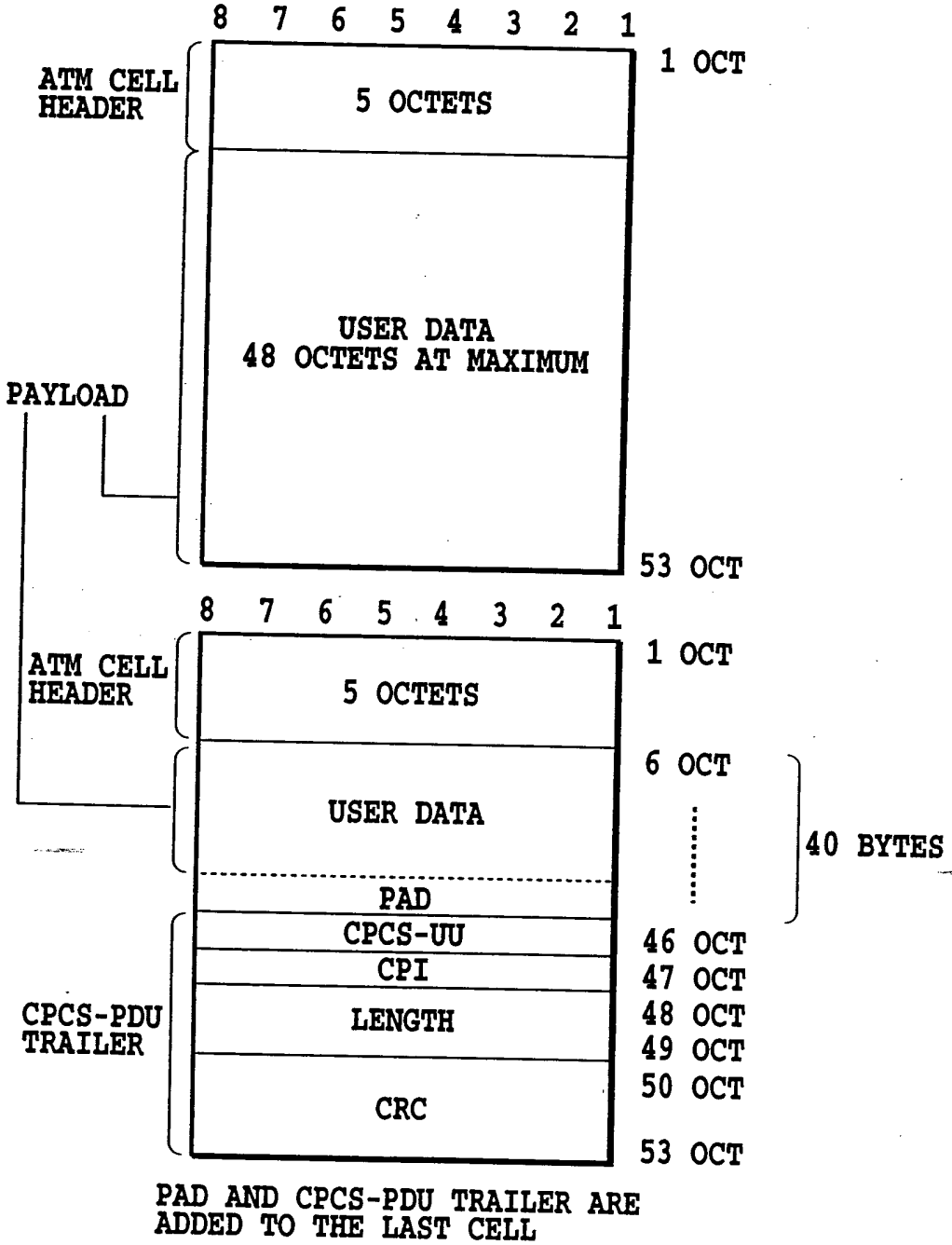

8 7 6 5 4 3 2 1
ATM CELL HEADER
5 OCTETS
1 OCT
USER DATA
48 OCTETS AT MAXIMUM
PAYLOAD
53 OCT
8 7 6 5 4 3 2 1
ATM CELL HEADER
5 OCTETS
1 OCT
6 OCT
USER DATA
40 BYTES
PAD
CPCS-UU
CPI
LENGTH
CRC
CPCS-PDU TRAILER
46 OCT
47 OCT
48 OCT
49 OCT
50 OCT
53 OCT
PAD AND CPCS-PDU TRAILER ARE ADDED TO THE LAST CELL

FIG.37

FIG.38

FIG.38A

FIG.38B

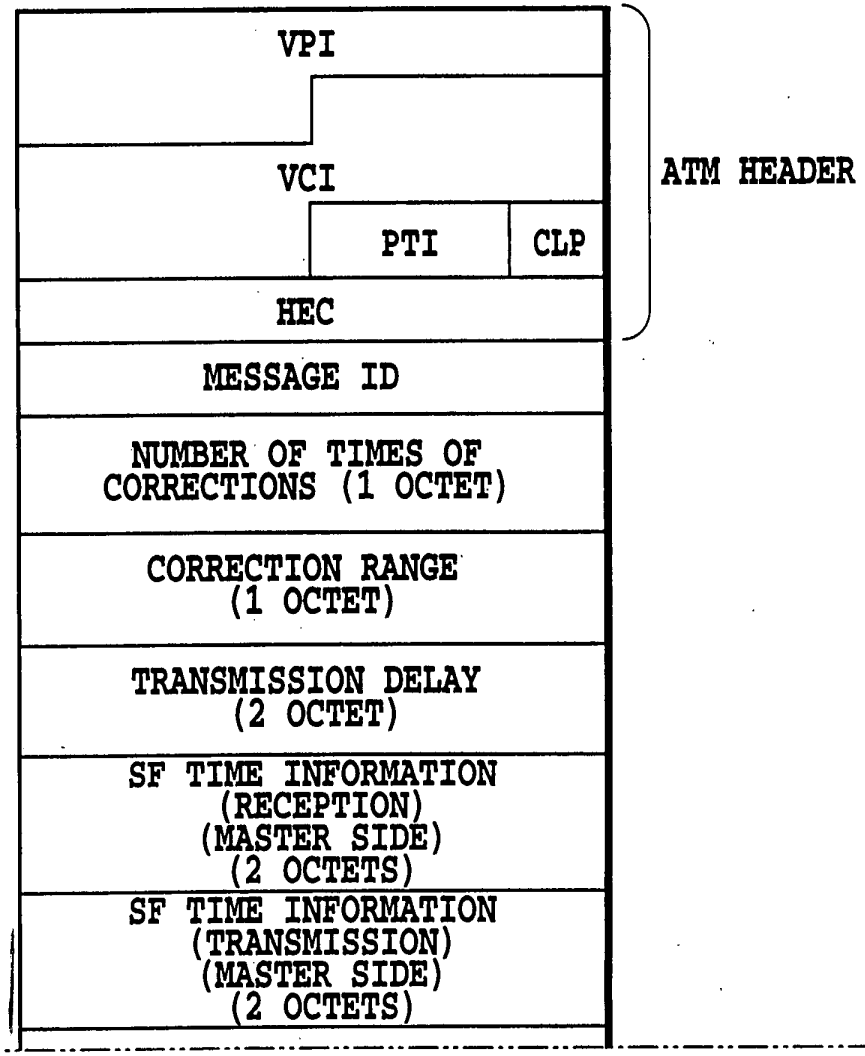


FIG.38A

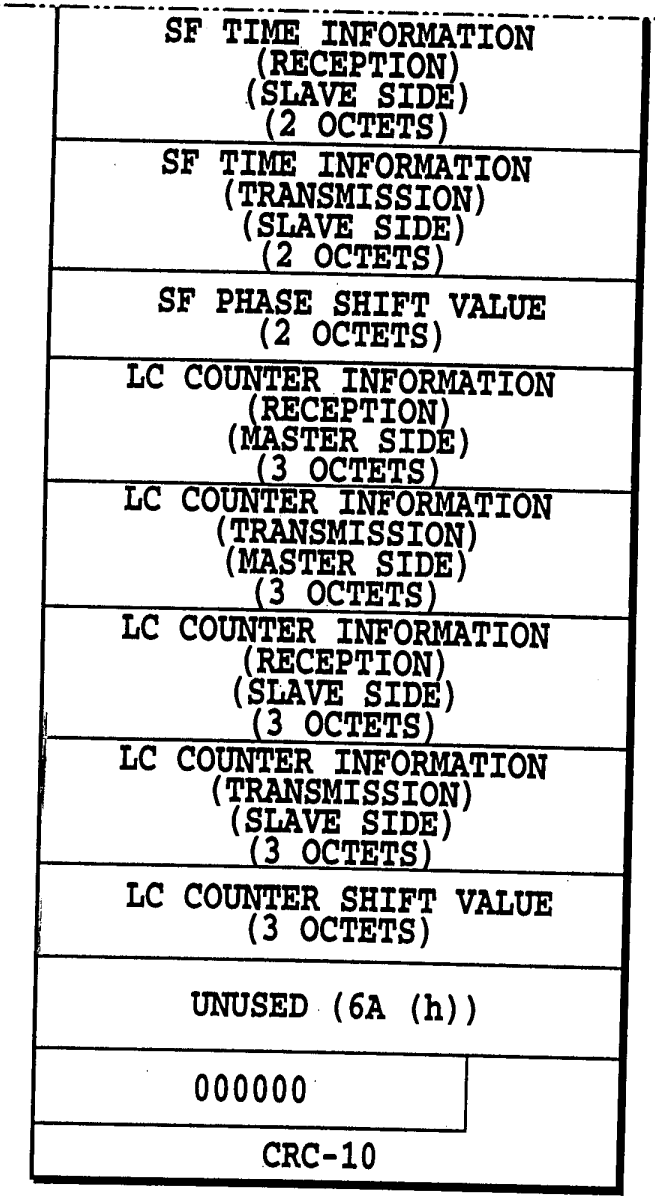

SF TIME INFORMATION (RECEPTION) (SLAVE SIDE) (2 OCTETS)
SF TIME INFORMATION (TRANSMISSION) (SLAVE SIDE) (2 OCTETS)
SF PHASE SHIFT VALUE (2 OCTETS)
LC COUNTER INFORMATION (RECEPTION) (MASTER SIDE) (3 OCTETS)
LC COUNTER INFORMATION (TRANSMISSION) (MASTER SIDE) (3 OCTETS)
LC COUNTER INFORMATION (RECEPTION) (SLAVE SIDE) (3 OCTETS)
LC COUNTER INFORMATION (TRANSMISSION) (SLAVE SIDE) (3 OCTETS)
LC COUNTER SHIFT VALUE (3 OCTETS)
UNUSED (6A (h))
000000
CRC-10

FIG.38B

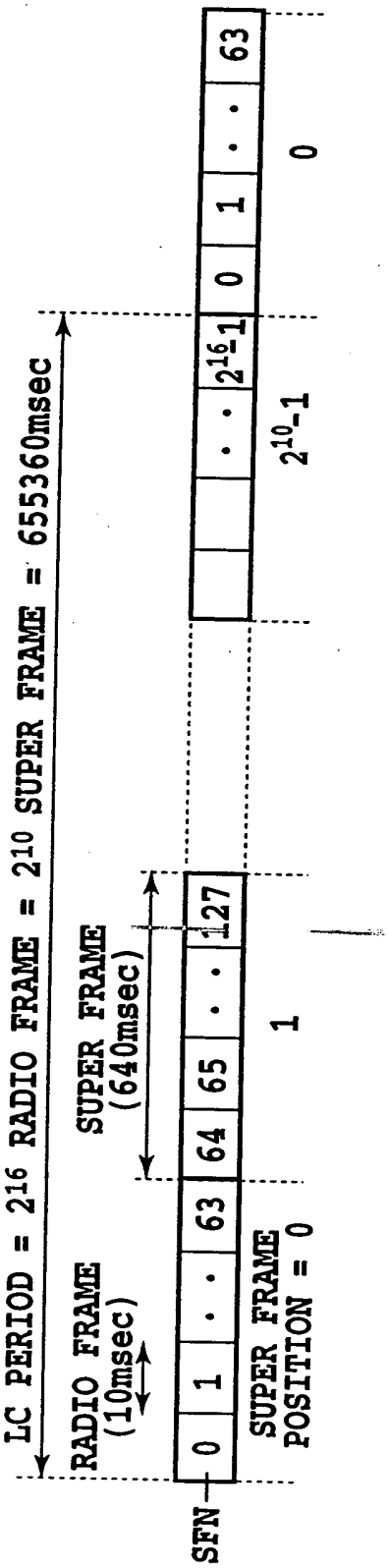

LC PERIOD = 2^16 RADIO FRAME = 2^10 SUPER FRAME = 655360msec
RADIO FRAME (10msec)
SUPER FRAME (640msec)
SUPER FRAME POSITION = 0
SFN
0
1
63
64
65
127
2^10-1
2^16-1

FIG.39

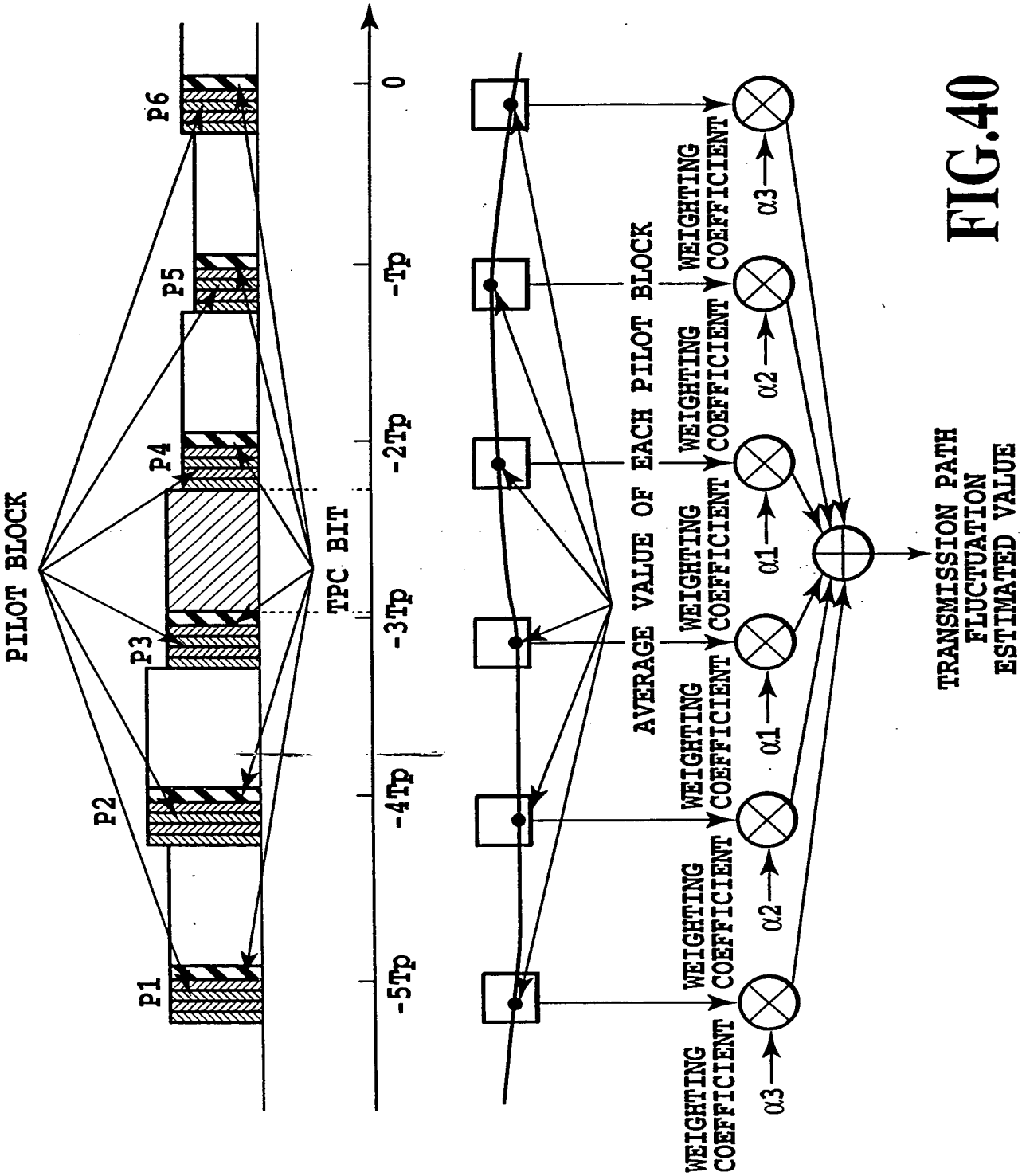
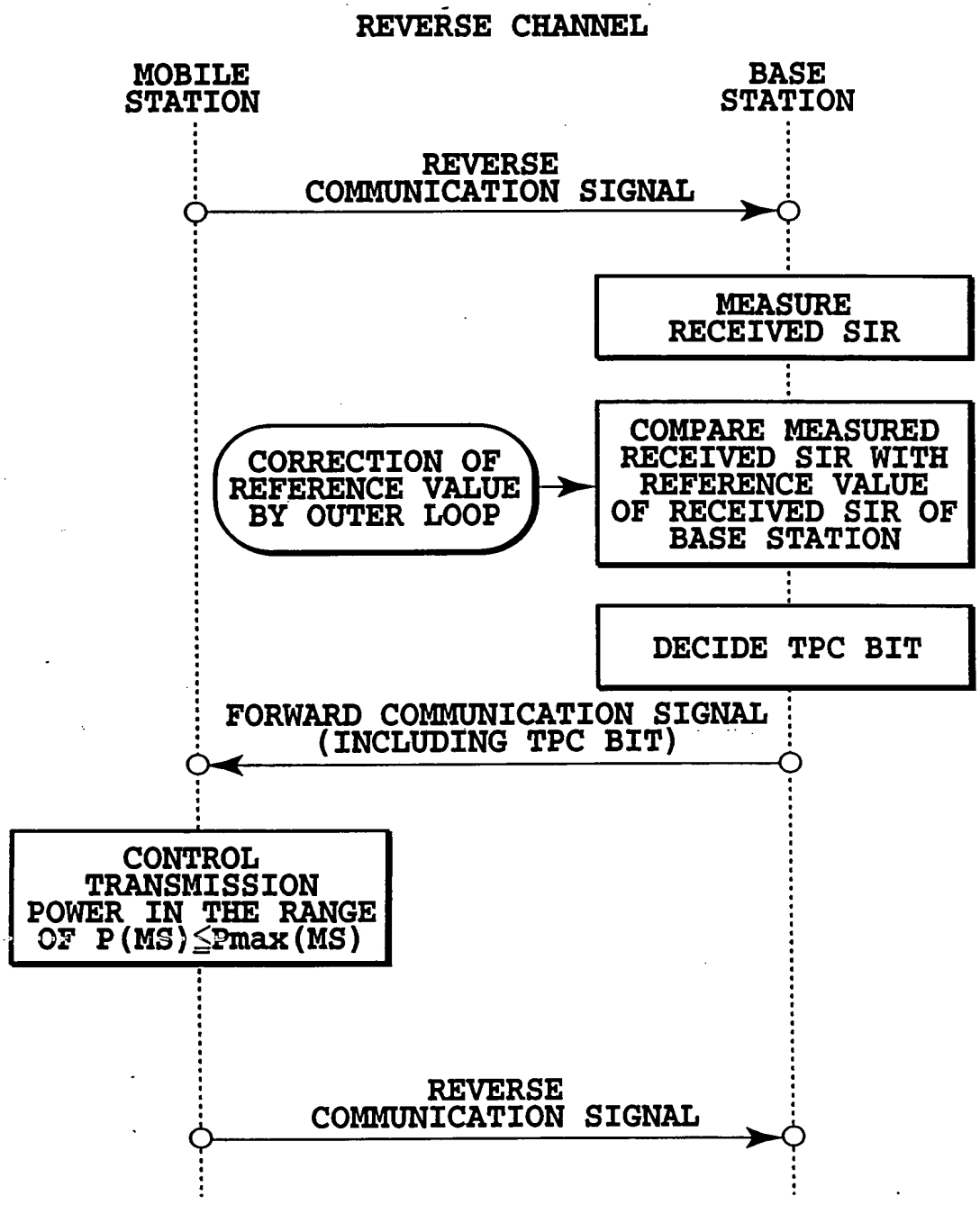

PILOT BLOCK
P1
P2
P3
P4
P5
P6
TPC BIT
0
-Tp
-2Tp
-3Tp
-4Tp
-5Tp
AVERAGE VALUE OF EACH PILOT BLOCK
WEIGHTING COEFFICIENT
WEIGHTING COEFFICIENT
WEIGHTING COEFFICIENT
WEIGHTING COEFFICIENT
WEIGHTING COEFFICIENT
α3
α2
α1
α1
α2
α3
TRANSMISSION PATH FLUCTUATION ESTIMATED VALUE

FIG.40



P(MS)• • •REVERSE TRANSMISSION POWER
Pmax(MS)• • •MAXIMUM REVERSE TRANSMISSION POWER
P(BS)• • •FORWARD TRANSMISSION POWER
Pmax(BS)• • •MAXIMUM FORWARD TRANSMISSION POWER
Pmin(BS)• • •MINIMUM FORWARD TRANSMISSION POWER

FIG.41A

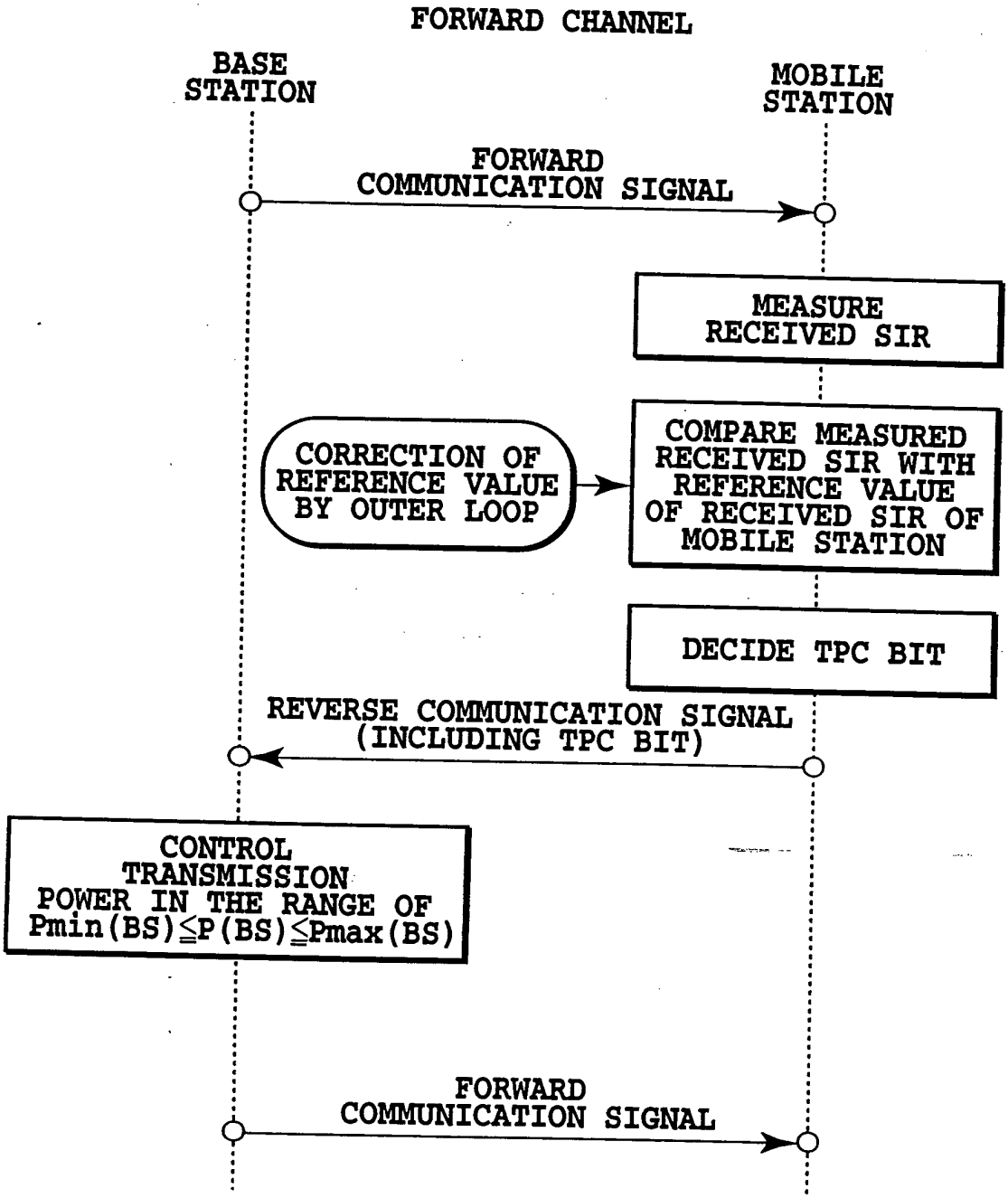

FORWARD CHANNEL
BASE STATION
MOBILE STATION
FORWARD COMMUNICATION SIGNAL
MEASURE RECEIVED SIR
CORRECTION OF REFERENCE VALUE BY OUTER LOOP
COMPARE MEASURED RECEIVED SIR WITH REFERENCE VALUE OF RECEIVED SIR OF MOBILE STATION
DECIDE TPC BIT
REVERSE COMMUNICATION SIGNAL (INCLUDING TPC BIT)
CONTROL TRANSMISSION POWER IN THE RANGE OF Pmin(BS)≦P(BS)≦Pmax(BS)
FORWARD COMMUNICATION SIGNAL

FIG.41B

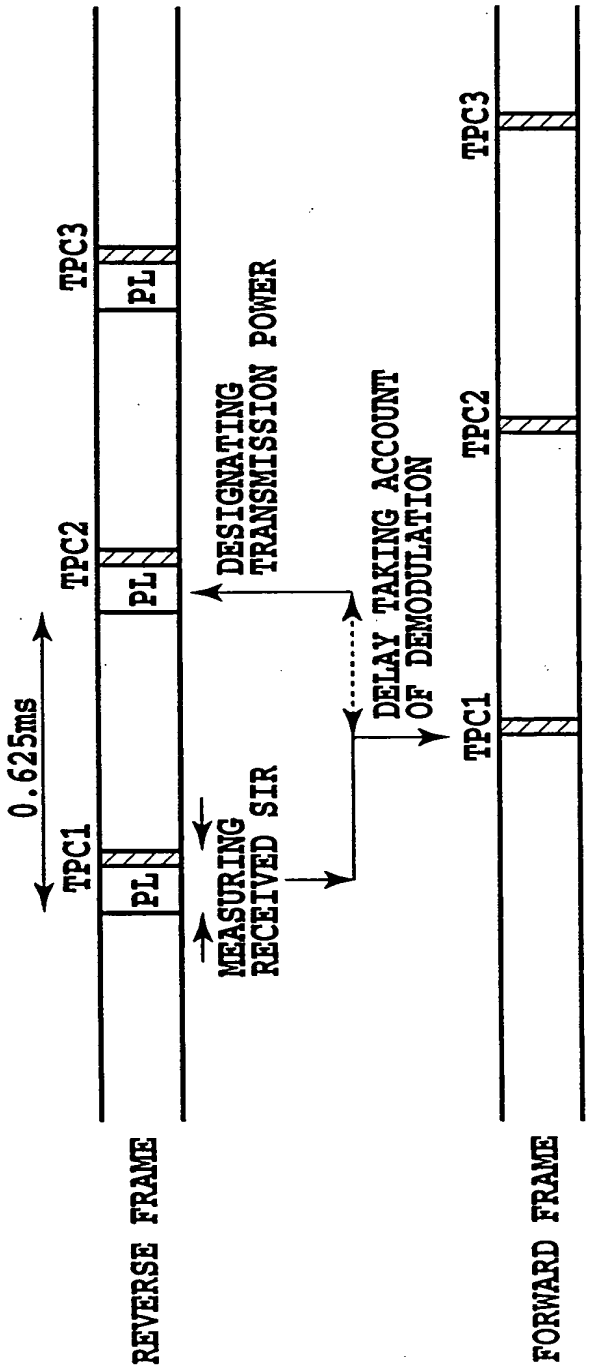

TPC3
PL
TPC2
PL
TPC1
PL
0.625ms
DESIGNATING TRANSMISSION POWER
MEASURING RECEIVED SIR
DELAY TAKING ACCOUNT OF DEMODULATION
TPC3
TPC2
TPC1
REVERSE FRAME
FORWARD FRAME

FIG.42

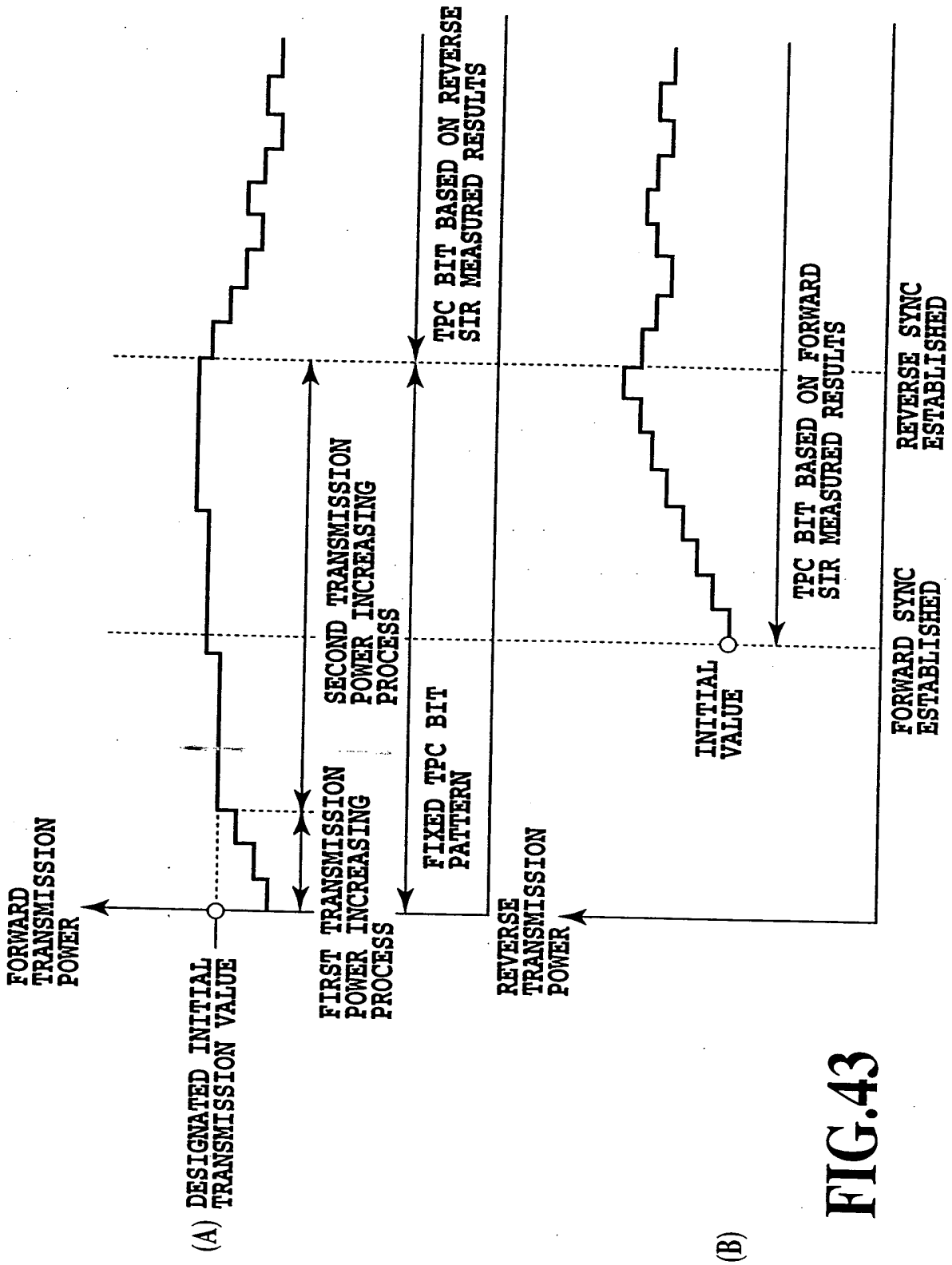
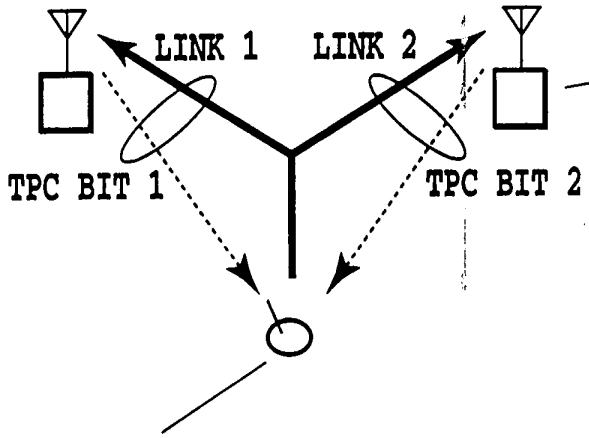

FORWARD TRANSMISSION POWER
(A) DESIGNATED INITIAL TRANSMISSION VALUE
FIRST TRANSMISSION POWER INCREASING PROCESS
SECOND TRANSMISSION POWER INCREASING PROCESS
FIXED TPC BIT PATTERN
TPC BIT BASED ON REVERSE SIR MEASURED RESULTS
REVERSE TRANSMISSION POWER
INITIAL VALUE
TPC BIT BASED ON FORWARD SIR MEASURED RESULTS
FORWARD SYNC ESTABLISHED
REVERSE SYNC ESTABLISHED
(B)

FIG.43



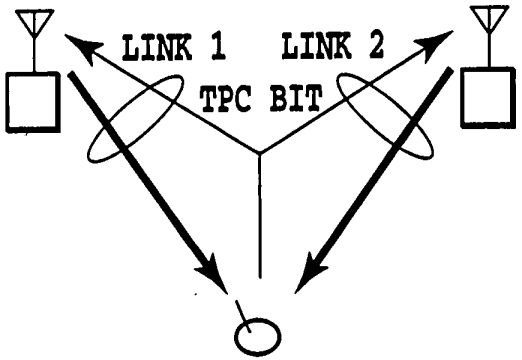
FUNCTIONS OF BASE STATION
(INDEPENDENT OF EACH OTHER BASE STATIONS)

- MEASURE REVERSE RECEIVED SIR
- DECIDE TPC BITS IN ACCORDANCE WITH MEASURED RESULTS OF RECEIVED SIR
- TRANSMIT TPC BITS TO MOBILE STATION

FUNCTIONS OF MOBILE STATION

- RECEIVE TPC BITS FROM MULTIPLE BASE STATIONS INDEPENDENTLY
- MEASURE RELIABILITY OF TPC BITS OF EACH BASE STATION
- DECIDE REVERSE TRANSMISSION POWER FROM TPC BITS OF EACH BASE STATION, AND CONTROL IT

FIG.44



FUNCTIONS OF BASE STATION
(INDEPENDENT OF EACH OTHER BASE STATIONS)

- RECEIVE TPC BITS
- CONTROL TRANSMISSION POWER IN RESPONSE TO TPC BITS

FUNCTIONS OF MOBILE STATION

- MEASURE RECEIVED SIR AFTER FORWARD SITE DIVERSITY COMBINING
- DECIDE TPC BITS IN ACCORDANCE WITH MEASURED RESULTS OF RECEIVED SIR

FIG.45

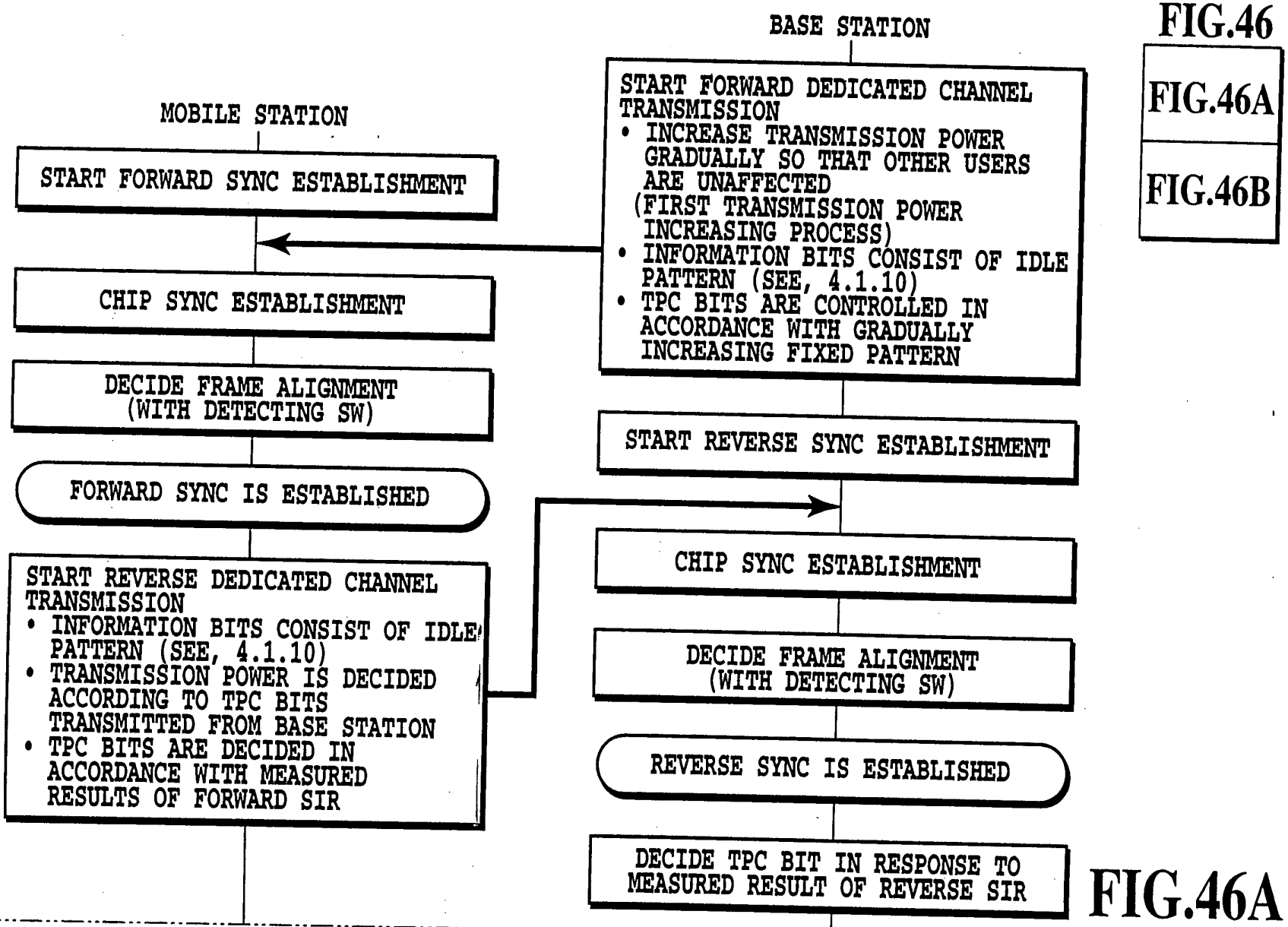


FIG.46

FIG.46A

FIG.46B

FIG.46A

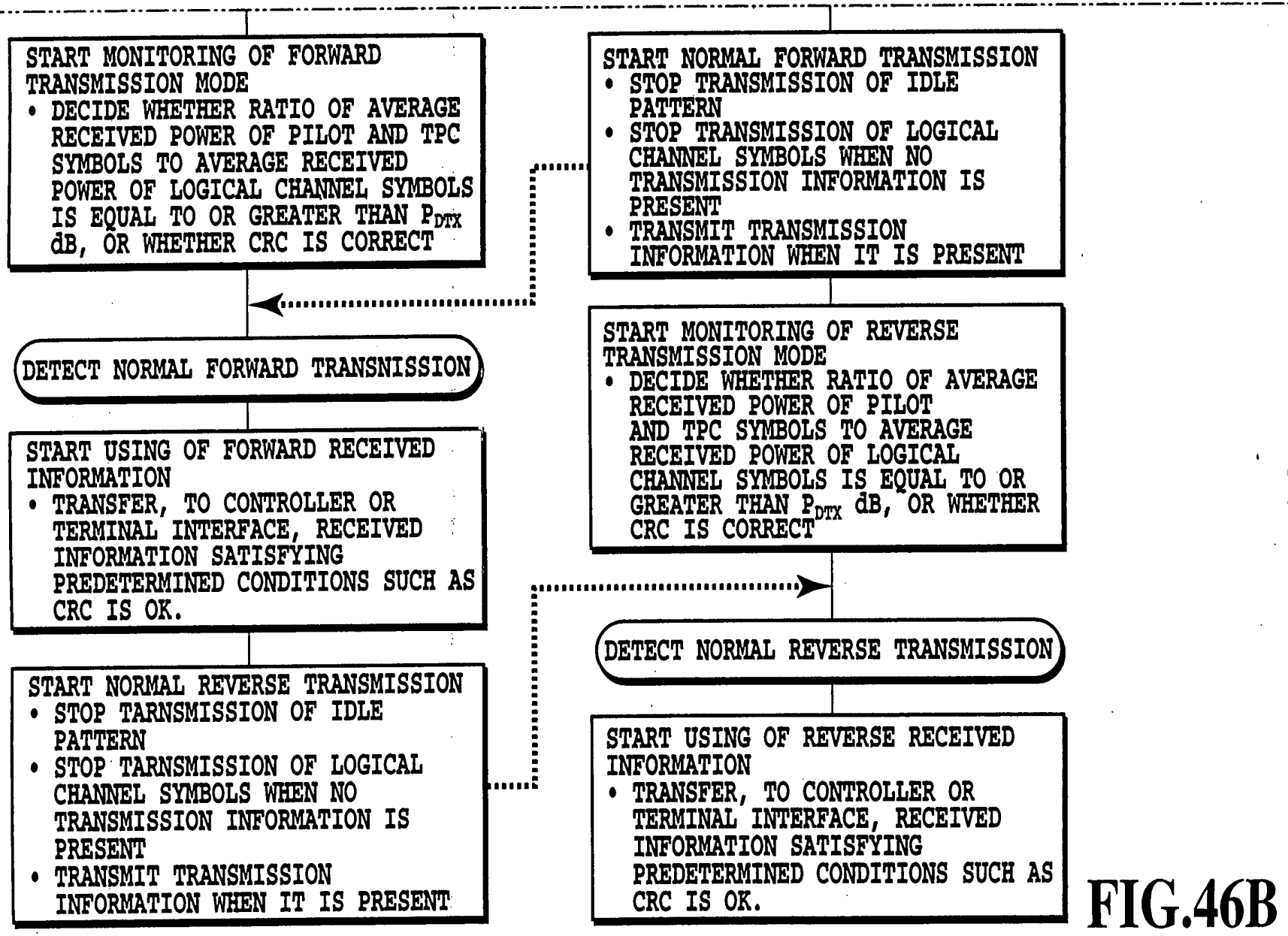

START MONITORING OF FORWARD TRANSMISSION MODE
• DECIDE WHETHER RATIO OF AVERAGE RECEIVED POWER OF PILOT AND TPC SYMBOLS TO AVERAGE RECEIVED POWER OF LOGICAL CHANNEL SYMBOLS IS EQUAL TO OR GREATER THAN P_{DTX} dB, OR WHETHER CRC IS CORRECT
DETECT NORMAL FORWARD TRANSNISSION
START USING OF FORWARD RECEIVED INFORMATION
• TRANSFER, TO CONTROLLER OR TERMINAL INTERFACE, RECEIVED INFORMATION SATISFYING PREDETERMINED CONDITIONS SUCH AS CRC IS OK.
START NORMAL REVERSE TRANSMISSION
• STOP TARNSMISSION OF IDLE PATTERN
• STOP TARNSMISSION OF LOGICAL CHANNEL SYMBOLS WHEN NO TRANSMISSION INFORMATION IS PRESENT
• TRANSMIT TRANSMISSION INFORMATION WHEN IT IS PRESENT
START NORMAL FORWARD TRANSMISSION
• STOP TRANSMISSION OF IDLE PATTERN
• STOP TRANSMISSION OF LOGICAL CHANNEL SYMBOLS WHEN NO TRANSMISSION INFORMATION IS PRESENT
• TRANSMIT TRANSMISSION INFORMATION WHEN IT IS PRESENT
START MONITORING OF REVERSE TRANSMISSION MODE
• DECIDE WHETHER RATIO OF AVERAGE RECEIVED POWER OF PILOT AND TPC SYMBOLS TO AVERAGE RECEIVED POWER OF LOGICAL CHANNEL SYMBOLS IS EQUAL TO OR GREATER THAN P_{DTX} dB, OR WHETHER CRC IS CORRECT
DETECT NORMAL REVERSE TRANSMISSION
START USING OF REVERSE RECEIVED INFORMATION
• TRANSFER, TO CONTROLLER OR TERMINAL INTERFACE, RECEIVED INFORMATION SATISFYING PREDETERMINED CONDITIONS SUCH AS CRC IS OK.

FIG.46B

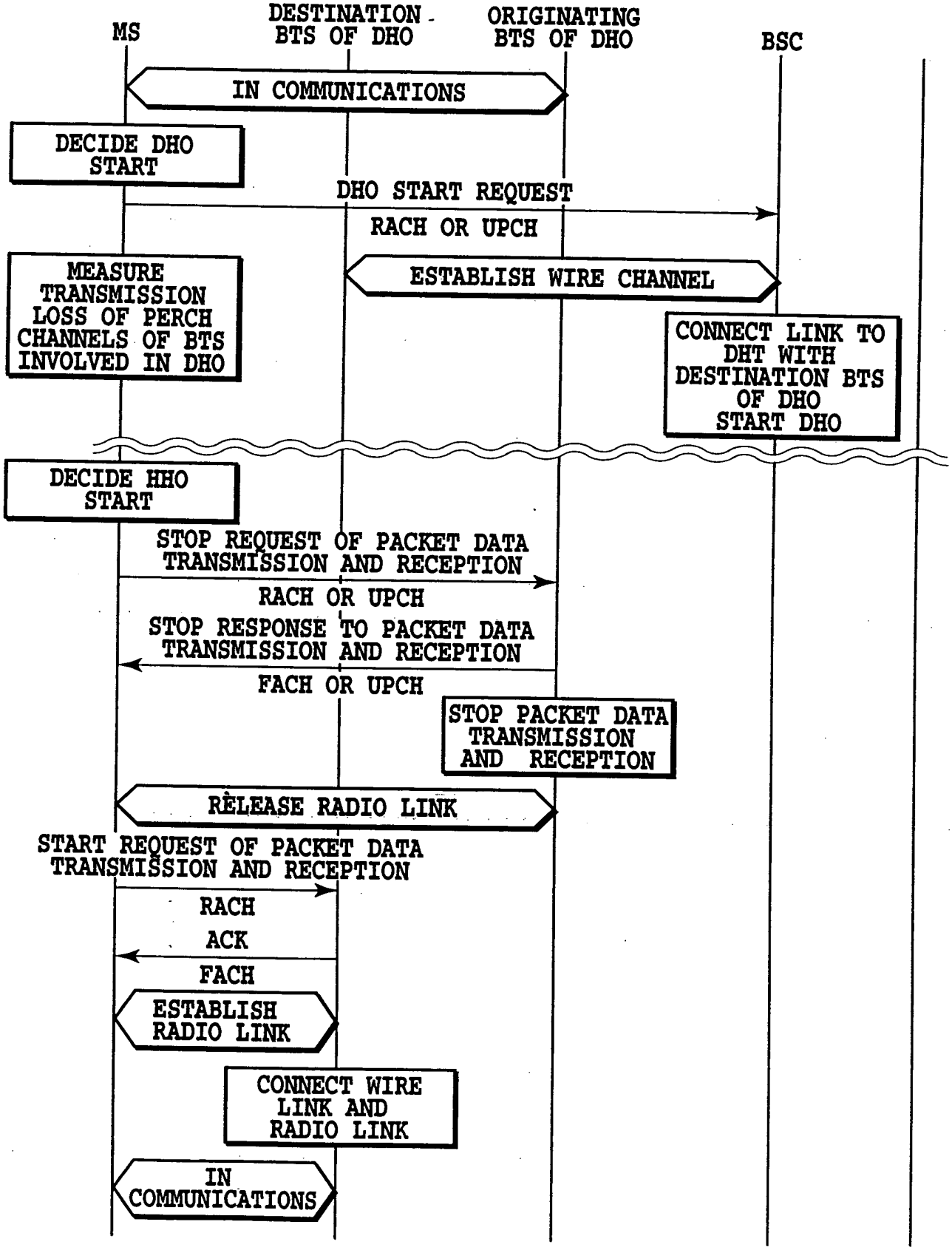
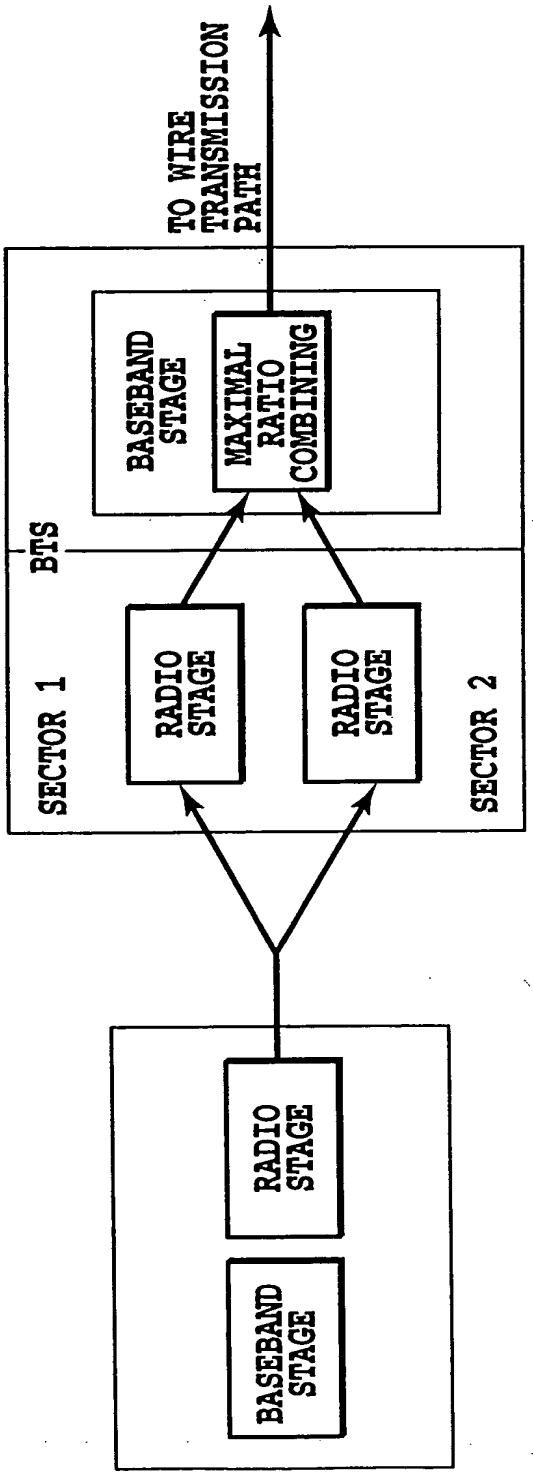
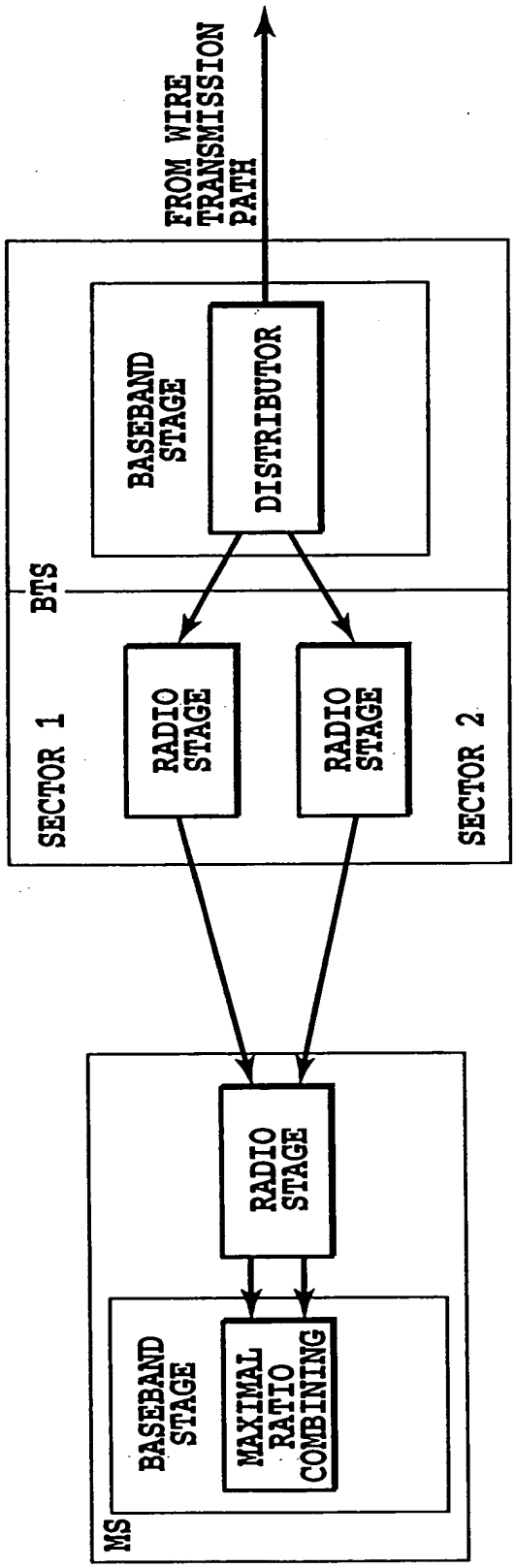

MS
DESTINATION BTS OF DHO
ORIGINATING BTS OF DHO
BSC
IN COMMUNICATIONS
DECIDE DHO START
DHO START REQUEST
RACH OR UPCH
MEASURE TRANSMISSION LOSS OF PERCH CHANNELS OF BTS INVOLVED IN DHO
ESTABLISH WIRE CHANNEL
CONNECT LINK TO DHT WITH DESTINATION BTS OF DHO START DHO
DECIDE HHO START
STOP REQUEST OF PACKET DATA TRANSMISSION AND RECEPTION
RACH OR UPCH
STOP RESPONSE TO PACKET DATA TRANSMISSION AND RECEPTION
FACH OR UPCH
STOP PACKET DATA TRANSMISSION AND RECEPTION
RELEASE RADIO LINK
START REQUEST OF PACKET DATA TRANSMISSION AND RECEPTION
RACH
ACK
FACH
ESTABLISH RADIO LINK
CONNECT WIRE LINK AND RADIO LINK
IN COMMUNICATIONS

FIG.47



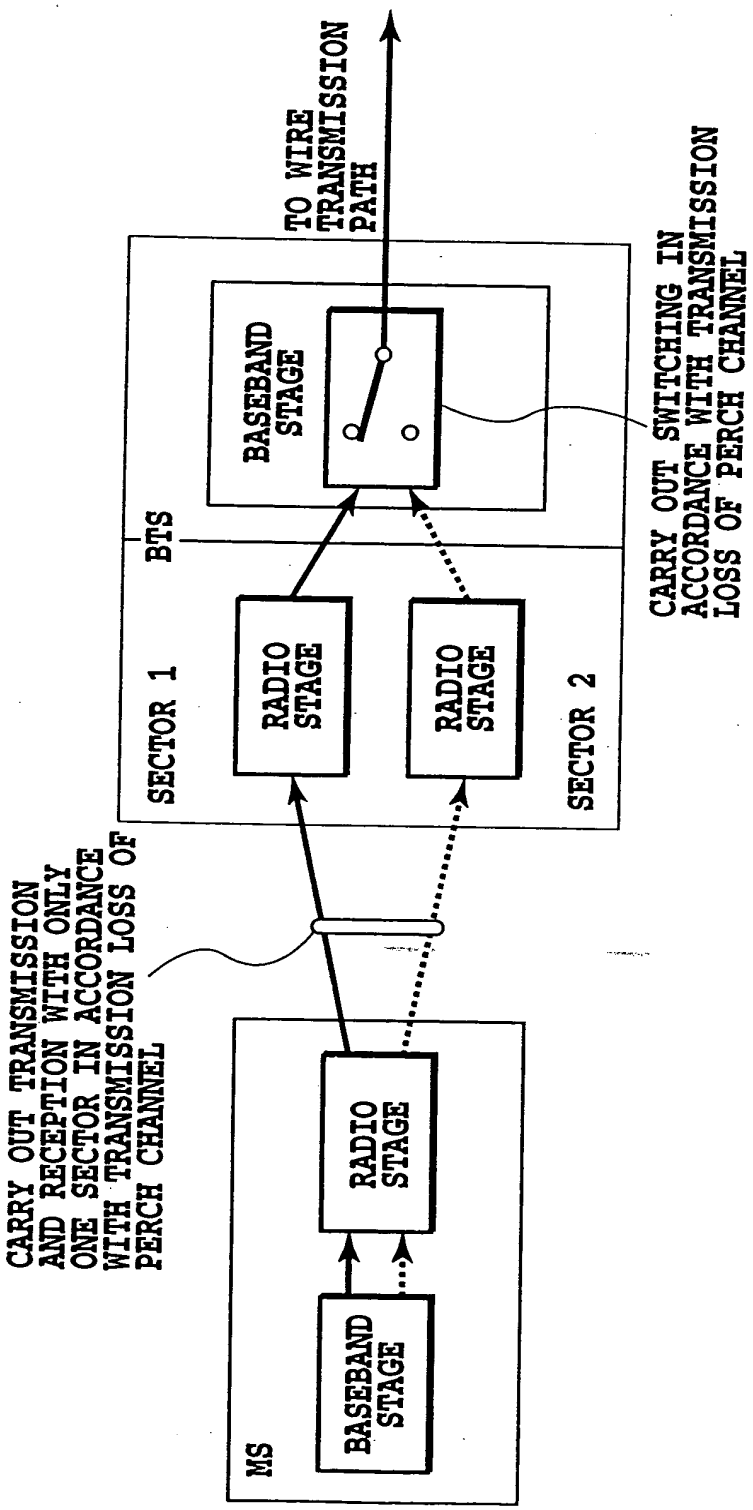
REVERSE DEDICATED PHYSICAL CHANNEL (UPCH)

FIG.48



FORWARD DEDICATED PHYSICAL CHANNEL (UPCH)

FIG.49



REVERSE COMMON CONTROL PHYSICAL CHANNEL (RACH)

FIG.50

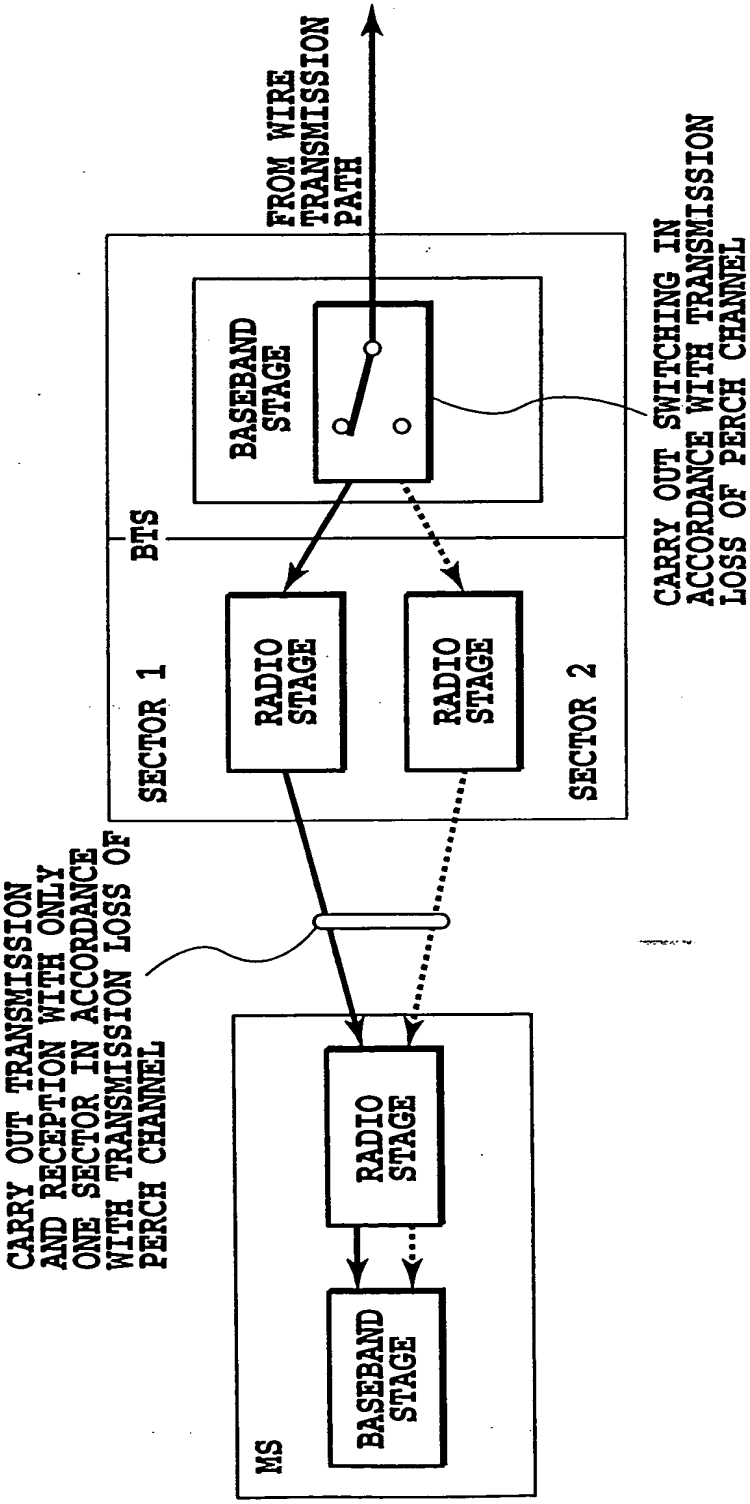

FROM WIRE TRANSMISSION PATH
BASEBAND STAGE
BTS
SECTOR 1
RADIO STAGE
RADIO STAGE
SECTOR 2
CARRY OUT SWITCHING IN ACCORDANCE WITH TRANSMISSION LOSS OF PERCH CHANNEL
CARRY OUT TRANSMISSION AND RECEPTION WITH ONLY ONE SECTOR IN ACCORDANCE WITH TRANSMISSION LOSS OF PERCH CHANNEL
MS
RADIO STAGE
BASEBAND STAGE
FORWARD COMMON CONTROL PHYSICAL CHANNEL (FACH)

FIG.51

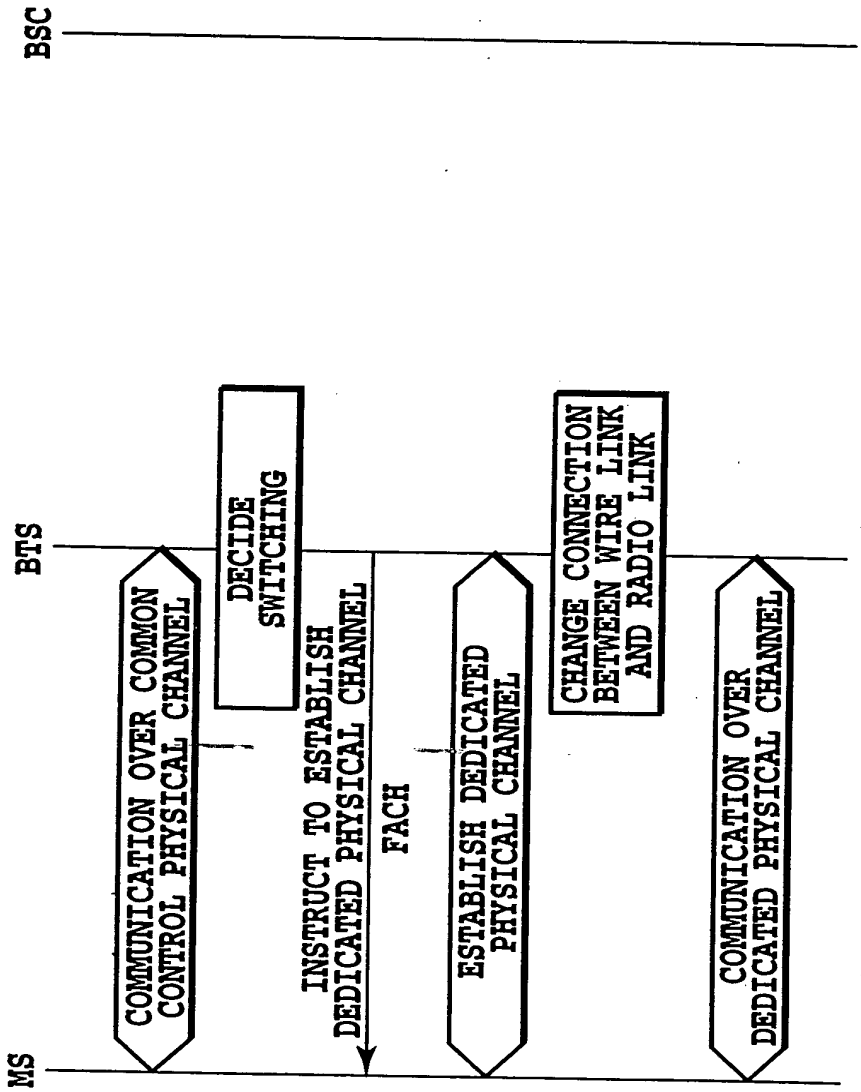

BSC
BTS
MS
COMMUNICATION OVER COMMON CONTROL PHYSICAL CHANNEL
DECIDE SWITCHING
INSTRUCT TO ESTABLISH DEDICATED PHYSICAL CHANNEL
FACH
ESTABLISH DEDICATED PHYSICAL CHANNEL
CHANGE CONNECTION BETWEEN WIRE LINK AND RADIO LINK
COMMUNICATION OVER DEDICATED PHYSICAL CHANNEL
FROM COMMON CONTROL PHYSICAL CHANNEL TO DEDICATED PHYSICAL CHANNEL

FIG.52

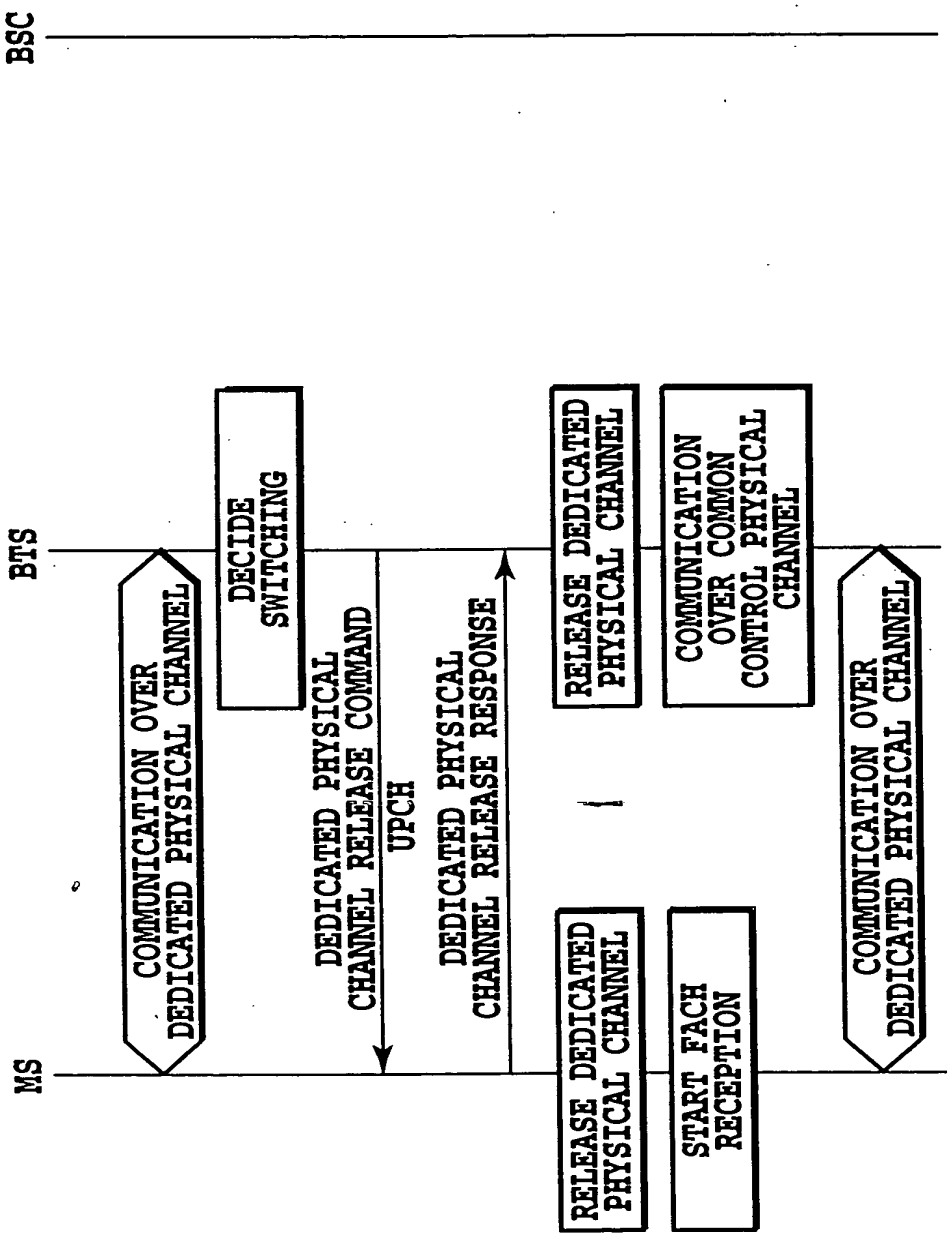

BSC
BTS
MS
COMMUNICATION OVER DEDICATED PHYSICAL CHANNEL
DECIDE SWITCHING
DEDICATED PHYSICAL CHANNEL RELEASE COMMAND
UPCH
DEDICATED PHYSICAL CHANNEL RELEASE RESPONSE
RELEASE DEDICATED PHYSICAL CHANNEL
COMMUNICATION OVER COMMON CONTROL PHYSICAL CHANNEL
RELEASE DEDICATED PHYSICAL CHANNEL
START FACH RECEPTION
COMMUNICATION OVER DEDICATED PHYSICAL CHANNEL
FROM DEDICATED PHYSICAL CHANNEL
TO COMMON CONTROL PHYSICAL CHANNEL

FIG.53

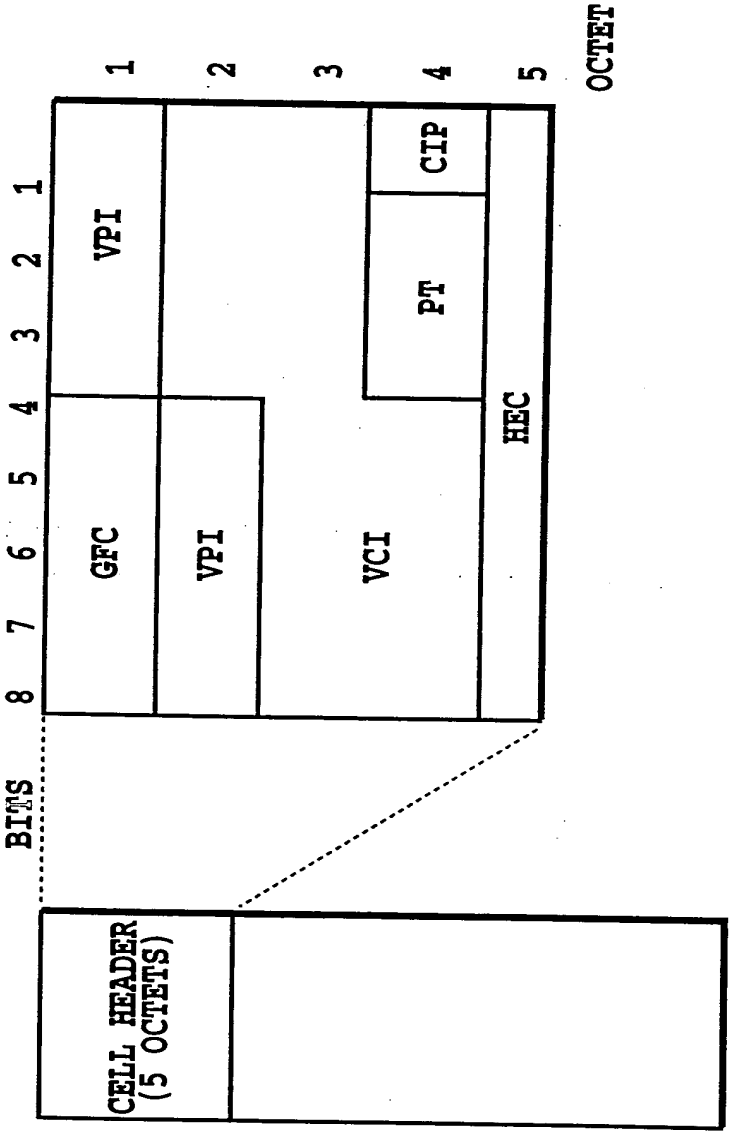

OCTET
1
2
3
4
5
BITS
1
2
3
4
5
6
7
8
VPI
CIP
PT
GFC
VPI
VCI
HEC
CELL HEADER
(5 OCTETS)

FIG.54

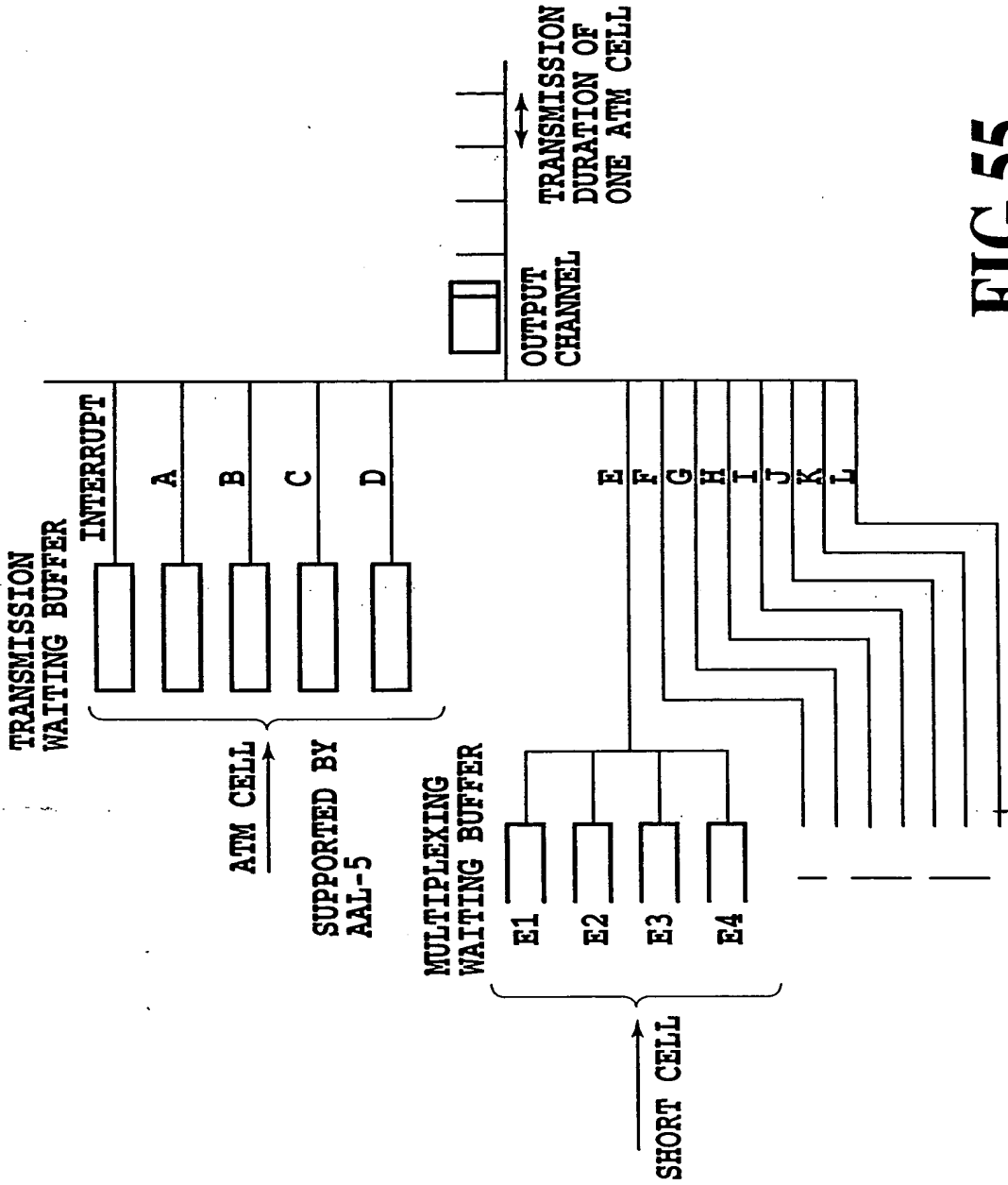

TRANSMISSION WAITING BUFFER
INTERRUPT
A
B
C
D
E
F
G
H
I
J
K
L
OUTPUT CHANNEL
TRANSMISSION DURATION OF ONE ATM CELL
ATM CELL
SUPPORTED BY AAL-5
MULTIPLEXING WAITING BUFFER
E1
E2
E3
E4
SHORT CELL

FIG.55

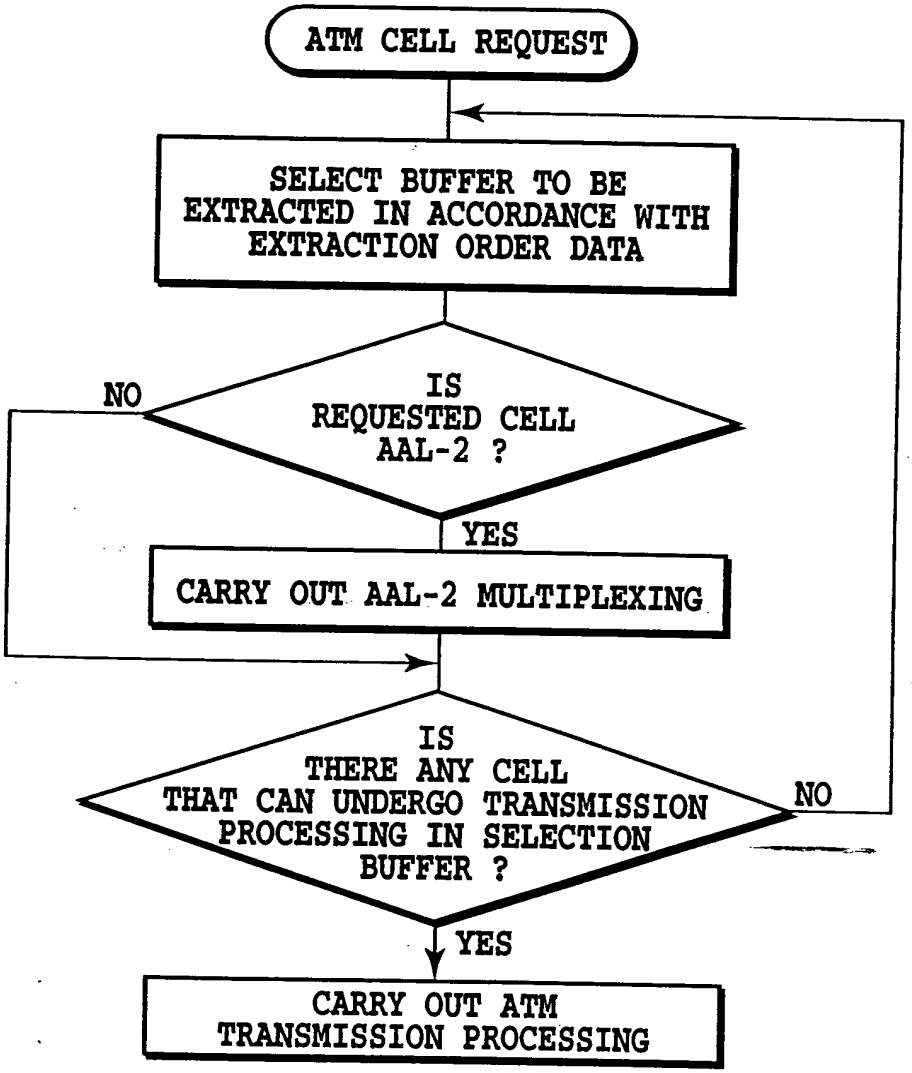

ATM CELL REQUEST
SELECT BUFFER TO BE EXTRACTED IN ACCORDANCE WITH EXTRACTION ORDER DATA
IS REQUESTED CELL AAL-2 ?
NO
YES
CARRY OUT AAL-2 MULTIPLEXING
IS THERE ANY CELL THAT CAN UNDERGO TRANSMISSION PROCESSING IN SELECTION BUFFER ?
NO
YES
CARRY OUT ATM TRANSMISSION PROCESSING

FIG.56

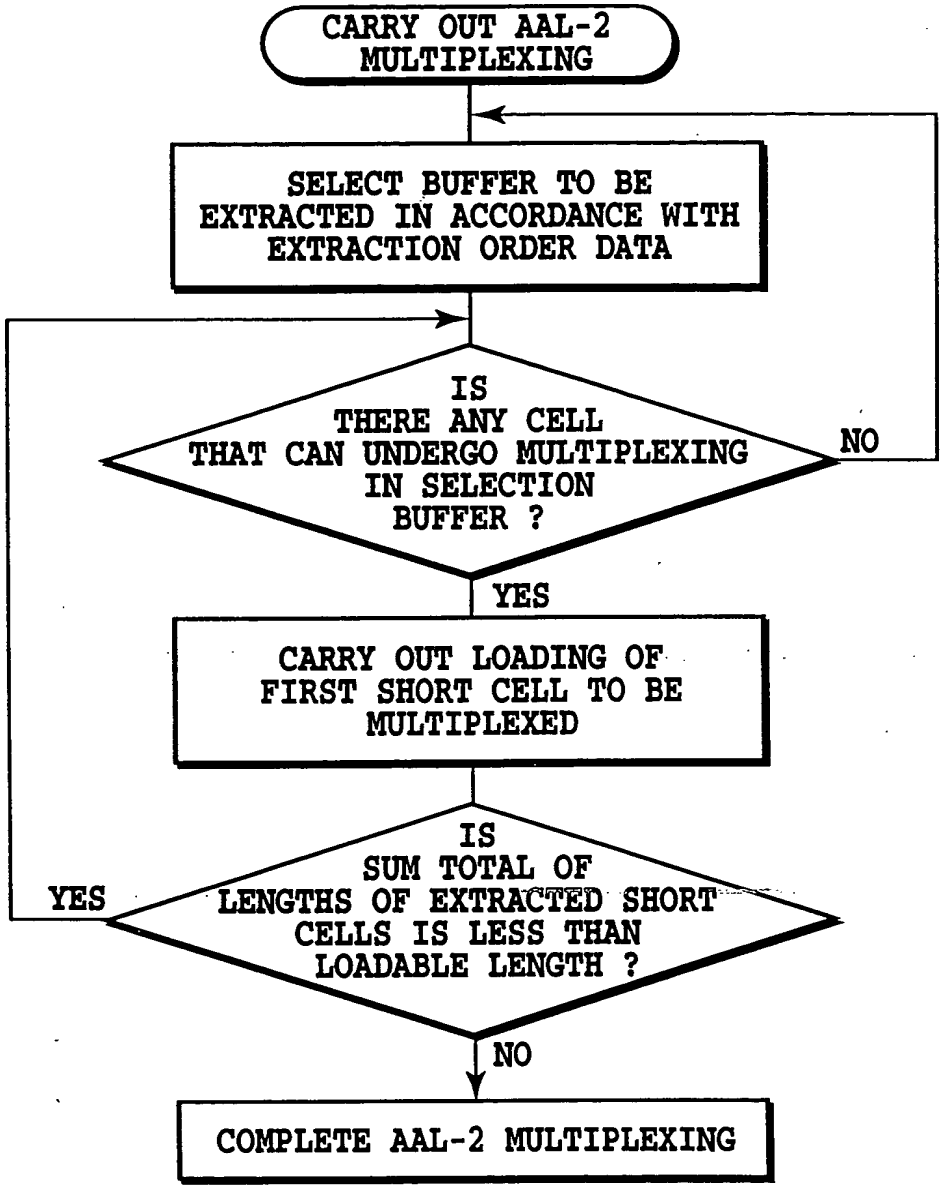

CARRY OUT AAL-2 MULTIPLEXING
SELECT BUFFER TO BE EXTRACTED IN ACCORDANCE WITH EXTRACTION ORDER DATA
IS THERE ANY CELL THAT CAN UNDERGO MULTIPLEXING IN SELECTION BUFFER ?
NO
YES
CARRY OUT LOADING OF FIRST SHORT CELL TO BE MULTIPLEXED
IS SUM TOTAL OF LENGTHS OF EXTRACTED SHORT CELLS IS LESS THAN LOADABLE LENGTH ?
YES
NO
COMPLETE AAL-2 MULTIPLEXING

FIG.57

ATM CELL TRANSMISSION SEQUENCE TABLE

TRANSMISSION ORDER (ABOUT 256 AT MAXIMUM) →

PRIORITY ↓

E	F	A	E	F	B	E	F	C	E	• • •
F	A	B	F	A	C	F	A	D	F	• • •
A	B	C	A	B	D	A	B	E	A	• • •
B	C	D	B	C	E	B	C	F	B	• • •
C	D	E	C	D	F	C	D	A	C	• • •
D	E	F	D	E	A	D	E	B	D	• • •

FIG.58A

SHORT CELL TRANSMISSION SEQUENCE TABLE
(QUALITY CLASS (6))

TRANSMISSION ORDER (ABOUT 128 AT MAXIMUM) →

PRIORITY ↓

E1	E1	E1	E2	E1	E1	E1	E3	• • •
E2	E2	E2	E3	E2	E2	E2	E4	• • •
E3	E3	E3	E4	E3	E3	E3	E1	• • •
E4	E4	E4	E1	E4	E4	E4	E2	• • •

FIG.58B

SHORT CELL TRANSMISSION SEQUENCE TABLE
(QUALITY CLASS (7))

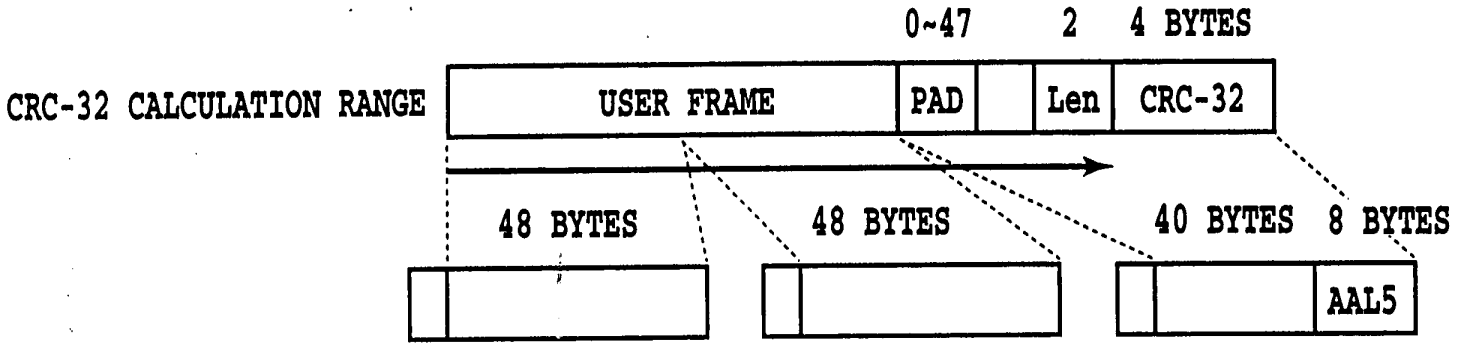
TRANSMISSION ORDER (ABOUT 128 AT MAXIMUM) →

PRIORITY ↓

F1	F1	F2	F1	F1	F3	F1	F1	• • •
F2	F2	F3	F2	F2	F4	F2	F2	• • •
F3	F3	F4	F3	F3	F1	F3	F3	• • •
F4	F4	F1	F4	F4	F2	F4	F4	• • •

FIG.58C

- CARRY OUT CELL EXTRACTION PROCESSING IN ACCORDANCE WITH TRANSMISSION SEQUENCE DETERMINED FOR EACH OUTPUT TIMING.
- IF NO CELL IS PRESENT IN HIGHER PRIORITY QUALITY CLASS, A CELL IN THE NEXT PRIORITY IS EXTRACTED.



PAD : PADDING BITS (ALL "0s")
Len : NUMBER OF BYTES OF EFFECTIVE DATA LENGTH OF USER FRAME
CRC-32 : CRC CHECKING BITS OVER 32 BITS
CRC-32 : GENERATOR POLYNOMIAL

$$G(X) = X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X^{1}+1$$

CHECK BITS ARE OBTAINED BY INVERTING BITS OF REMAINDER GENERATED BY THE GENERATOR POLYNOMIAL.

FIG.59

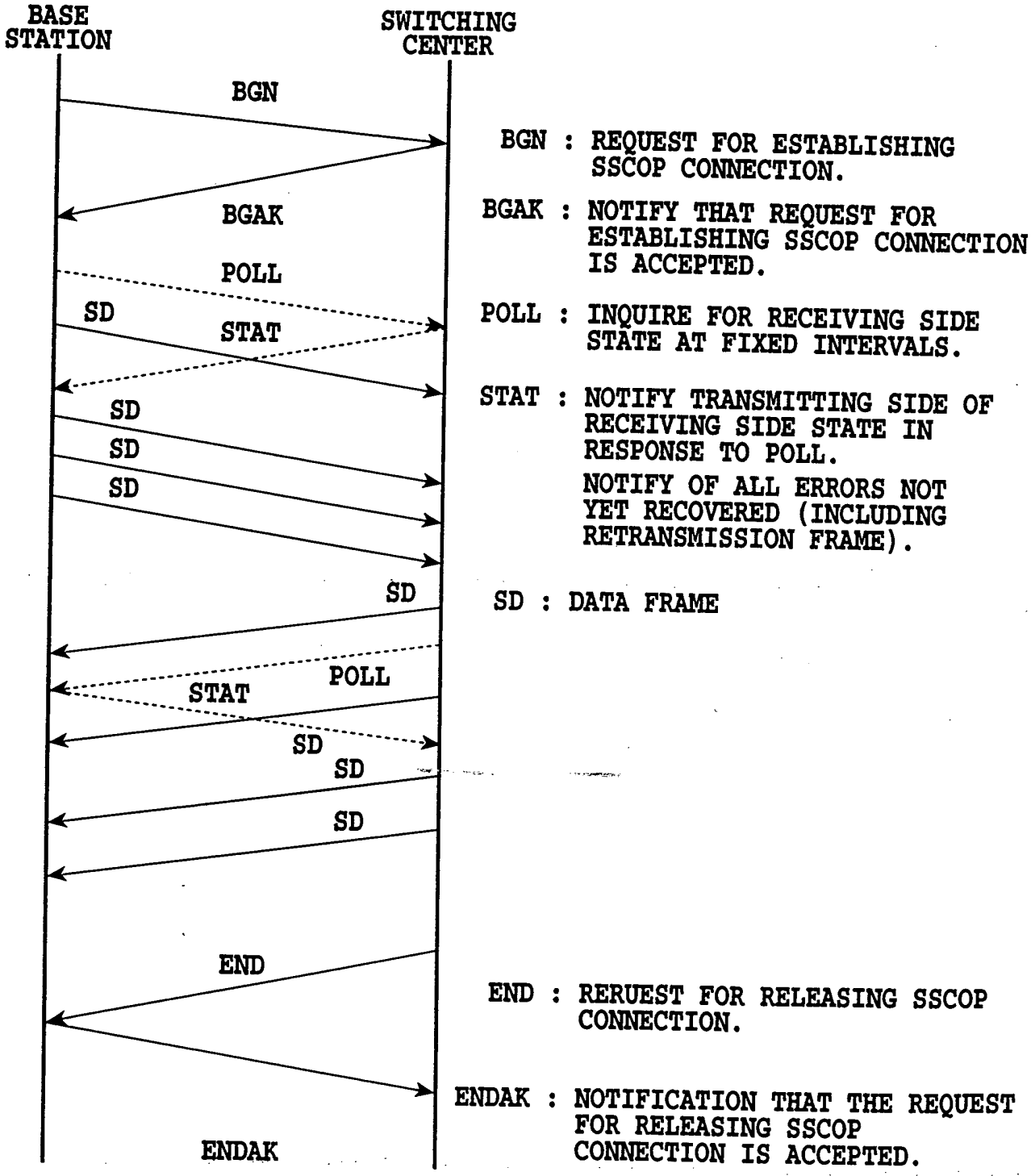

BASE STATION
SWITCHING CENTER
BGN
BGAK
POLL
SD
STAT
SD
SD
SD
SD
STAT
POLL
SD
SD
SD
END
ENDAK
BGN : REQUEST FOR ESTABLISHING SSCOP CONNECTION.
BGAK : NOTIFY THAT REQUEST FOR ESTABLISHING SSCOP CONNECTION IS ACCEPTED.
POLL : INQUIRE FOR RECEIVING SIDE STATE AT FIXED INTERVALS.
STAT : NOTIFY TRANSMITTING SIDE OF RECEIVING SIDE STATE IN RESPONSE TO POLL.
NOTIFY OF ALL ERRORS NOT YET RECOVERED (INCLUDING RETRANSMISSION FRAME).
SD : DATA FRAME
END : RERUEST FOR RELEASING SSCOP CONNECTION.
ENDAK : NOTIFICATION THAT THE REQUEST FOR RELEASING SSCOP CONNECTION IS ACCEPTED.

FIG.60

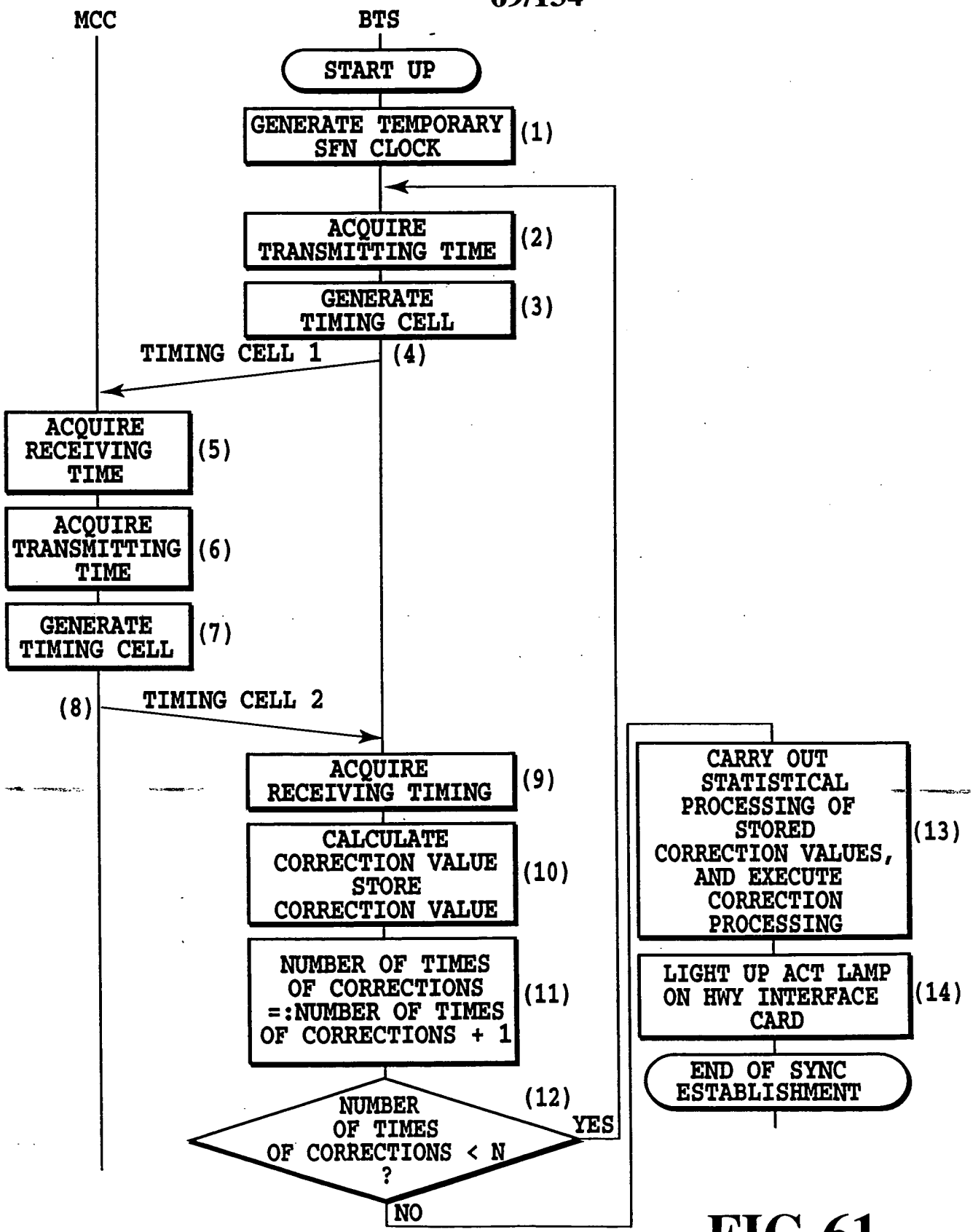

MCC
BTS
START UP
GENERATE TEMPORARY SFN CLOCK
(1)
ACQUIRE TRANSMITTING TIME
(2)
GENERATE TIMING CELL
(3)
TIMING CELL 1
(4)
ACQUIRE RECEIVING TIME
(5)
ACQUIRE TRANSMITTING TIME
(6)
GENERATE TIMING CELL
(7)
(8)
TIMING CELL 2
ACQUIRE RECEIVING TIMING
(9)
CALCULATE CORRECTION VALUE STORE CORRECTION VALUE
(10)
NUMBER OF TIMES OF CORRECTIONS =:NUMBER OF TIMES OF CORRECTIONS + 1
(11)
NUMBER OF TIMES OF CORRECTIONS < N ?
(12)
YES
NO
CARRY OUT STATISTICAL PROCESSING OF STORED CORRECTION VALUES, AND EXECUTE CORRECTION PROCESSING
(13)
LIGHT UP ACT LAMP ON HWY INTERFACE CARD
(14)
END OF SYNC ESTABLISHMENT

FIG 61

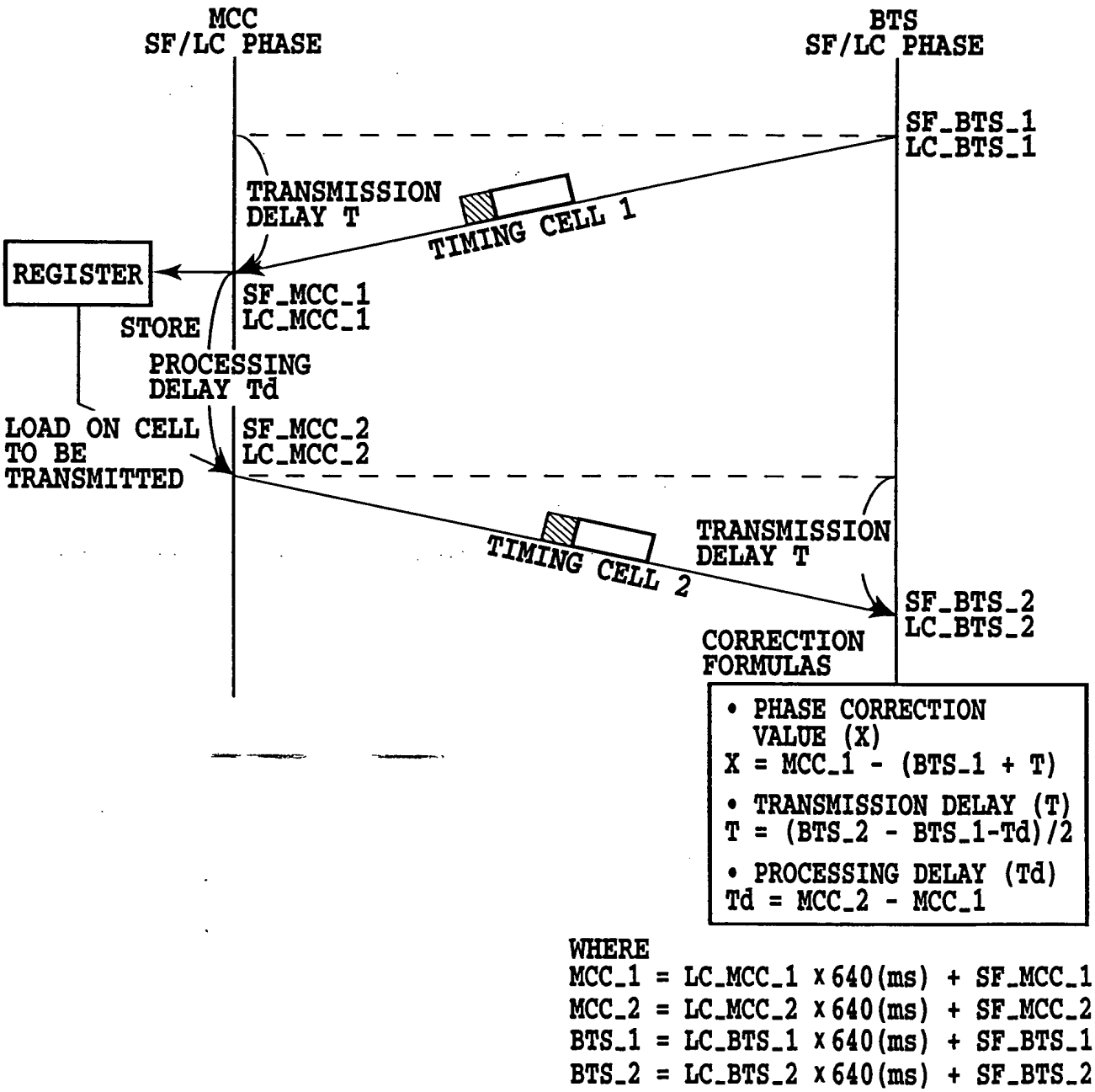

MCC
SF/LC PHASE
BTS
SF/LC PHASE
SF_BTS_1
LC_BTS_1
TRANSMISSION
DELAY T
TIMING CELL 1
REGISTER
SF_MCC_1
LC_MCC_1
STORE
PROCESSING
DELAY Td
LOAD ON CELL
TO BE
TRANSMITTED
SF_MCC_2
LC_MCC_2
TIMING CELL 2
TRANSMISSION
DELAY T
SF_BTS_2
LC_BTS_2
CORRECTION
FORMULAS
• PHASE CORRECTION
VALUE (X)
X = MCC_1 - (BTS_1 + T)
• TRANSMISSION DELAY (T)
T = (BTS_2 - BTS_1-Td)/2
• PROCESSING DELAY (Td)
Td = MCC_2 - MCC_1
WHERE
MCC_1 = LC_MCC_1 x 640(ms) + SF_MCC_1
MCC_2 = LC_MCC_2 x 640(ms) + SF_MCC_2
BTS_1 = LC_BTS_1 x 640(ms) + SF_BTS_1
BTS_2 = LC_BTS_2 x 640(ms) + SF_BTS_2

FIG.62

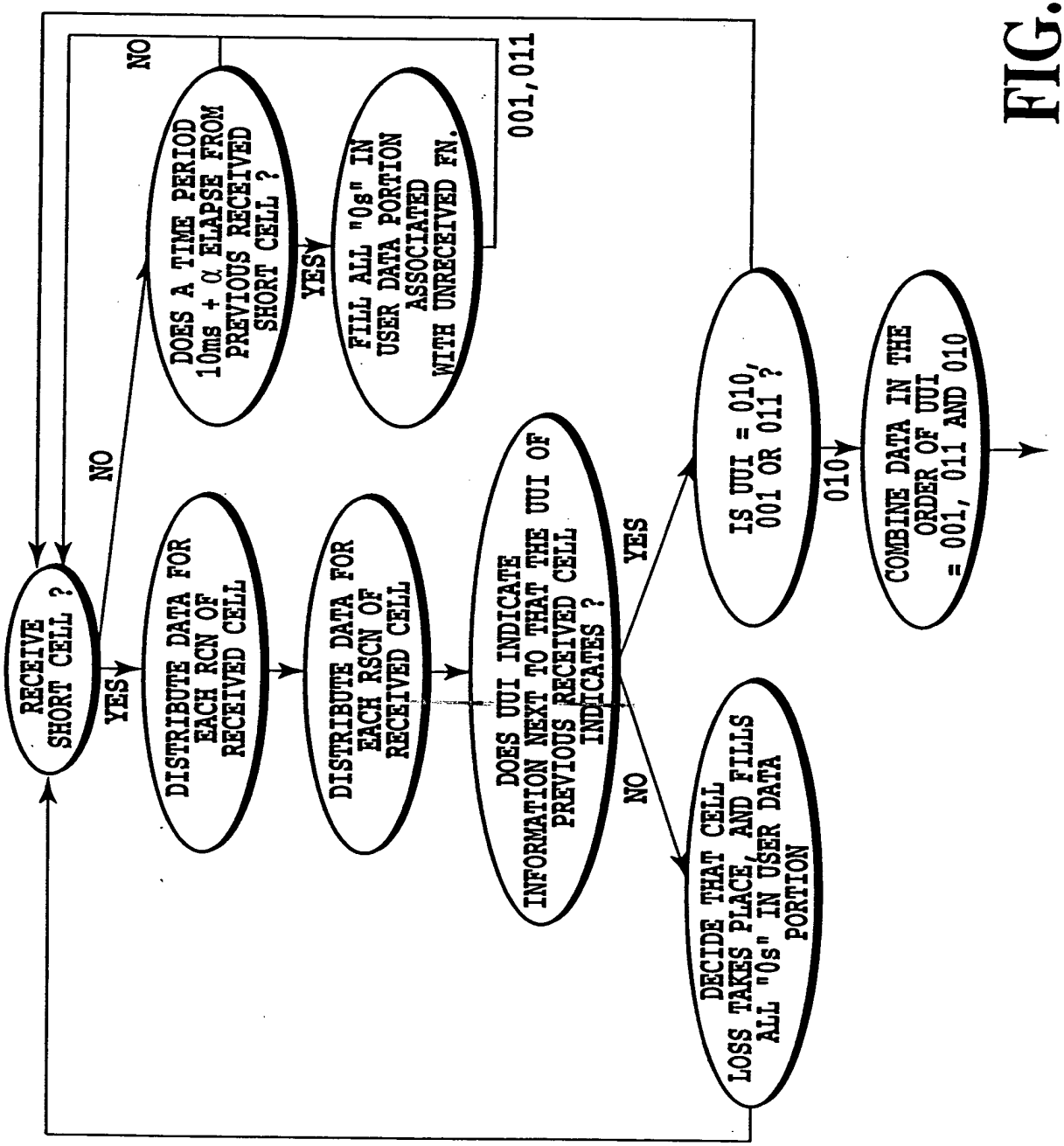

RECEIVE SHORT CELL ?
YES
NO
DISTRIBUTE DATA FOR EACH RCN OF RECEIVED CELL
DISTRIBUTE DATA FOR EACH RSCN OF RECEIVED CELL
DOES UUI INDICATE INFORMATION NEXT TO THAT THE UUI OF PREVIOUS RECEIVED CELL INDICATES ?
YES
NO
IS UUI = 010, 001 OR 011 ?
010
COMBINE DATA IN THE ORDER OF UUI = 001, 011 AND 010
DECIDE THAT CELL LOSS TAKES PLACE, AND FILLS ALL "0s" IN USER DATA PORTION
DOES A TIME PERIOD 10ms + α ELAPSE FROM PREVIOUS RECEIVED SHORT CELL ?
NO
YES
FILL ALL "0s" IN USER DATA PORTION ASSOCIATED WITH UNRECEIVED FN.
001,011

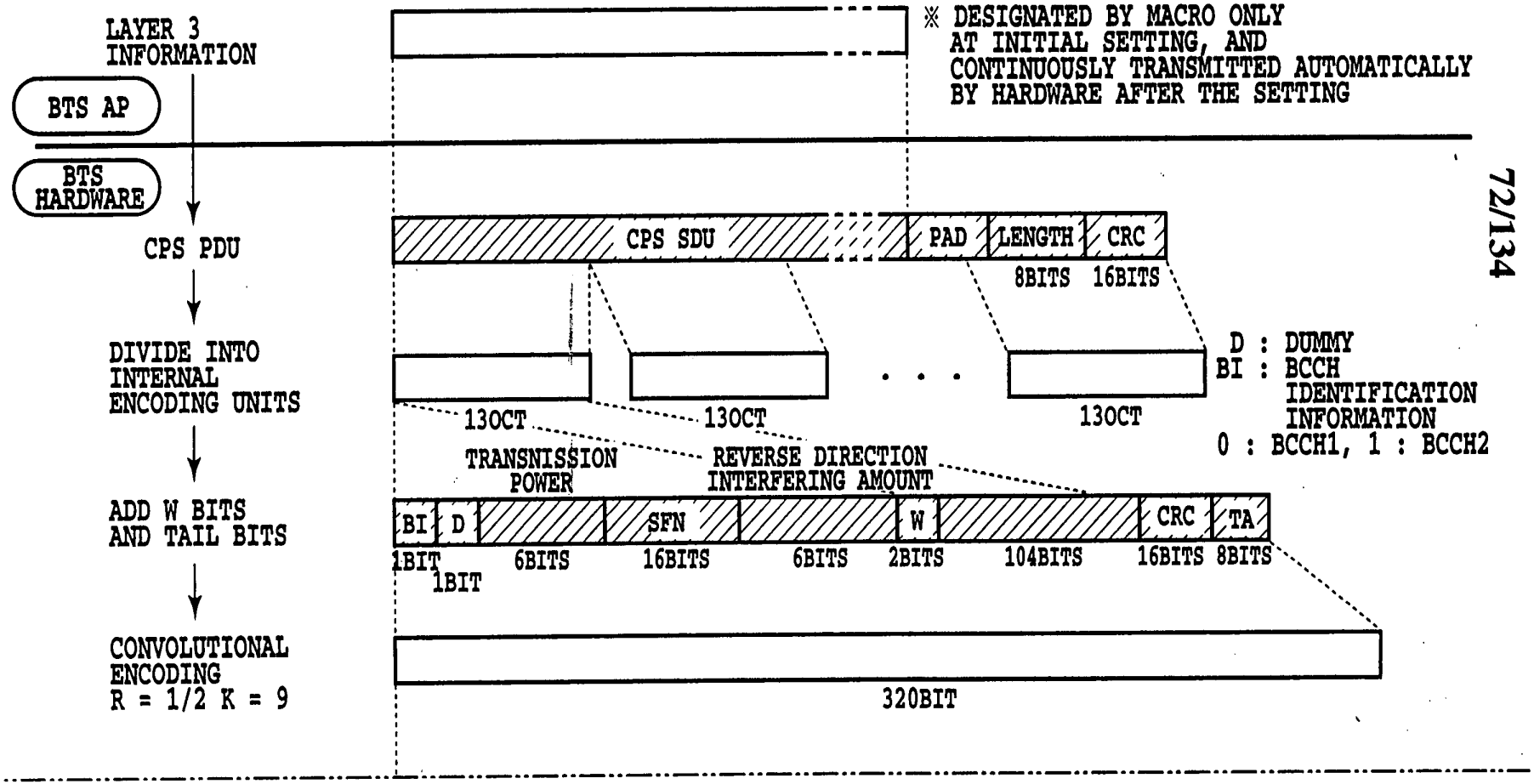
FIG.63

FIG.64

FIG.64A

FIG.64B

FIG.64A



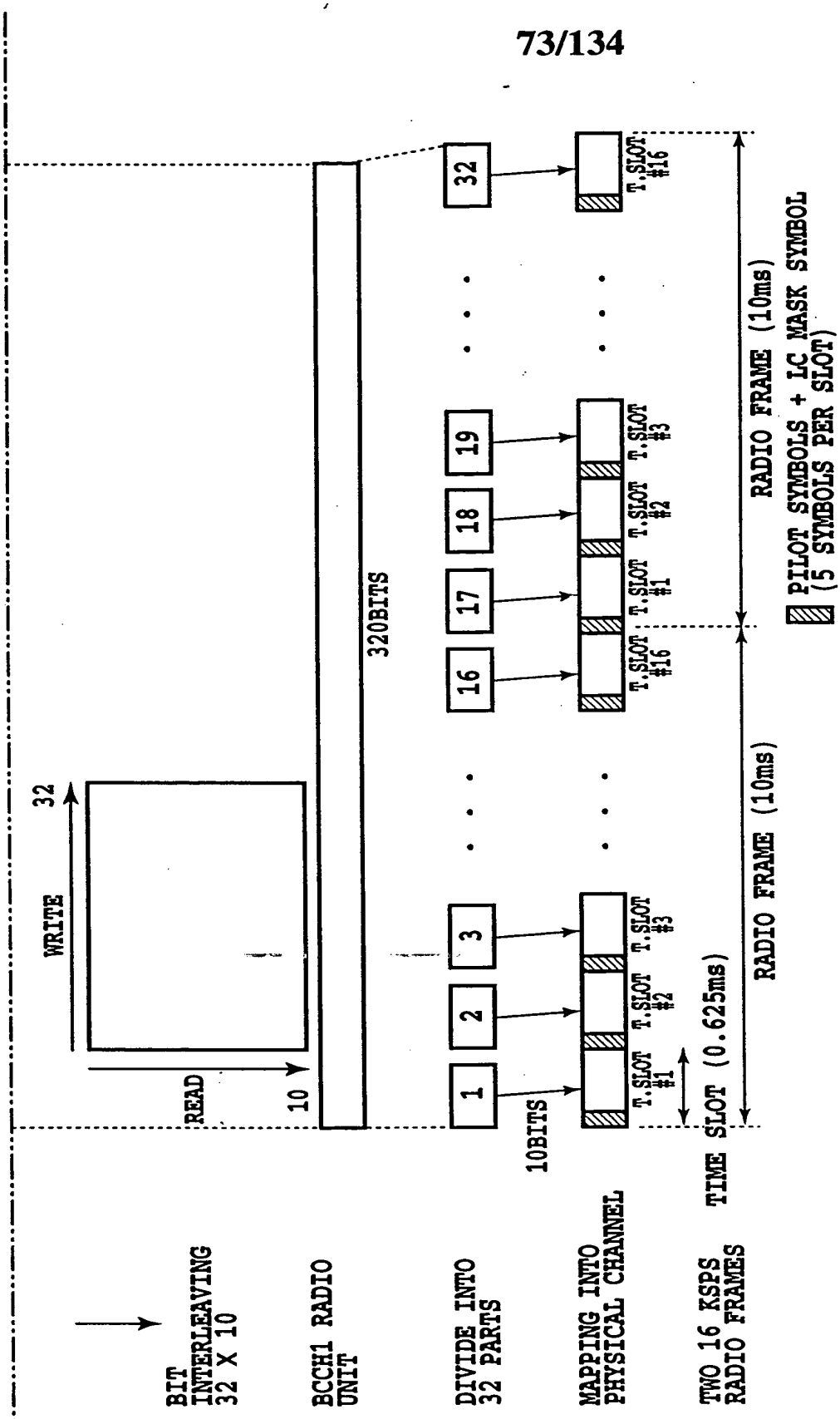

BIT INTERLEAVING 32 X 10
BCCH1 RADIO UNIT
DIVIDE INTO 32 PARTS
MAPPING INTO PHYSICAL CHANNEL
TWO 16 KSPS RADIO FRAMES
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
RADIO FRAME (10ms)
PILOT SYMBOLS + LC MASK SYMBOL (5 SYMBOLS PER SLOT)
WRITE
READ
32
10
320BITS
10BITS
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #16

FIG.64B

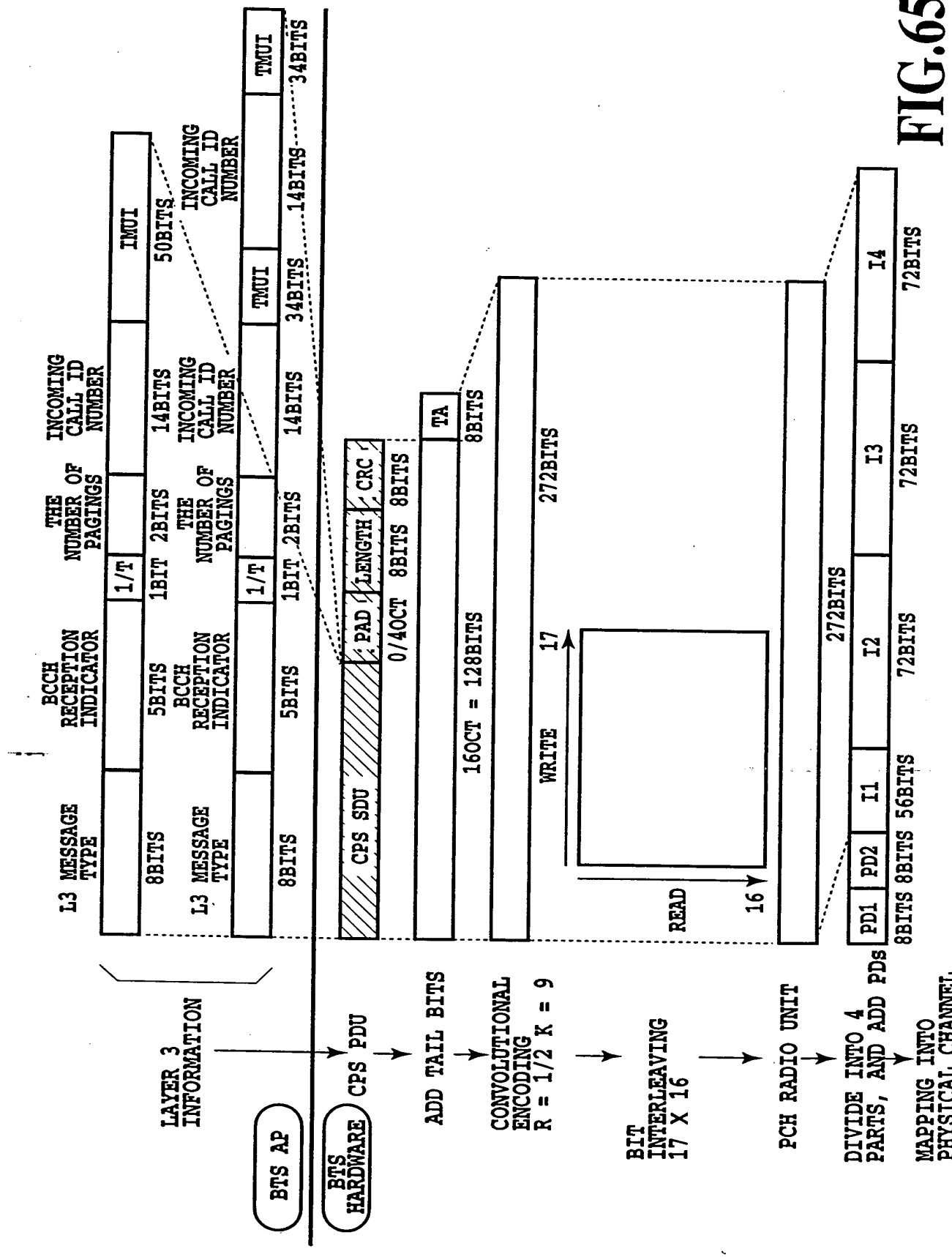

L3 MESSAGE TYPE
BCCH RECEPTION INDICATOR
1/T
THE NUMBER OF PAGINGS
INCOMING CALL ID NUMBER
IMUI
TMUI
8BITS
5BITS
1BIT
2BITS
14BITS
50BITS
34BITS
CPS SDU
PAD
LENGTH
CRC
0/40CT
8BITS
TA
160CT = 128BITS
272BITS
WRITE
17
16
READ
I1
I2
I3
I4
72BITS
56BITS
PD1
PD2
LAYER 3 INFORMATION
BTS AP
BTS HARDWARE
CPS PDU
ADD TAIL BITS
CONVOLUTIONAL ENCODING R = 1/2 K = 9
BIT INTERLEAVING 17 X 16
PCH RADIO UNIT
DIVIDE INTO 4 PARTS, AND ADD PDs
MAPPING INTO PHYSICAL CHANNEL 64 KSPS 6 TIME SLOT

FIG.65A

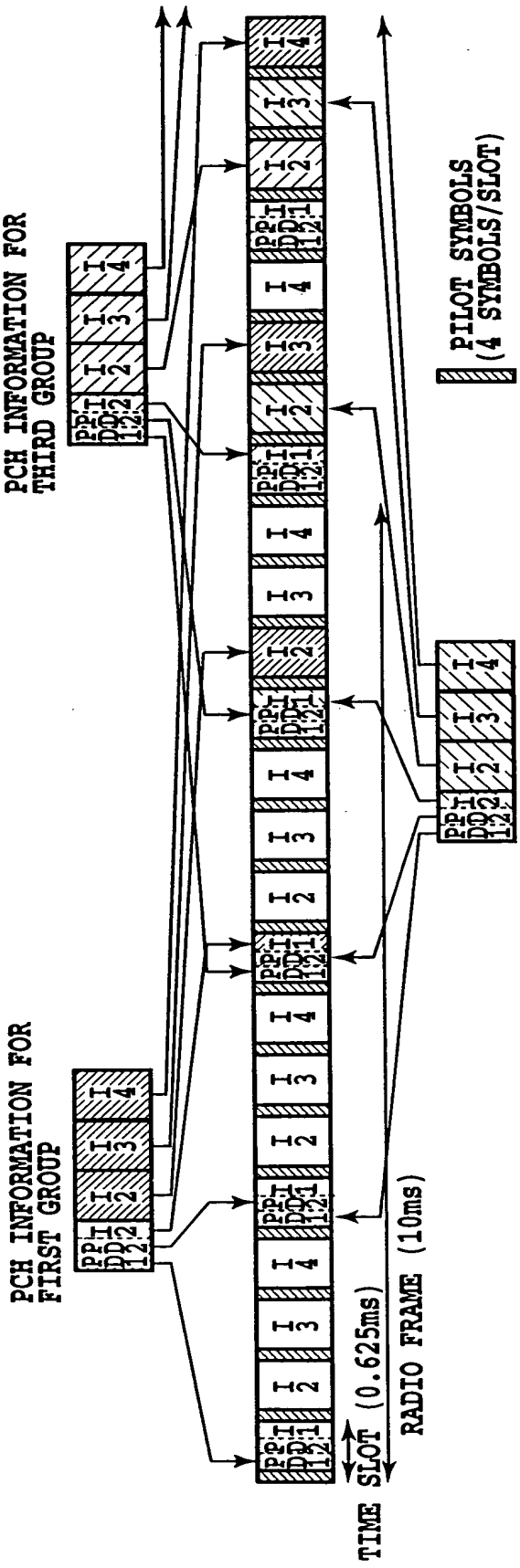

PCH INFORMATION FOR FIRST GROUP
PCH INFORMATION FOR THIRD GROUP
PCH INFORMATION FOR SECOND GROUP
PILOT SYMBOLS (4 SYMBOLS/SLOT)
TIME SLOT (0.625ms)
RADIO FRAME (10ms)

FIG.65B

FIG.66

FIG.66A

FIG.66B

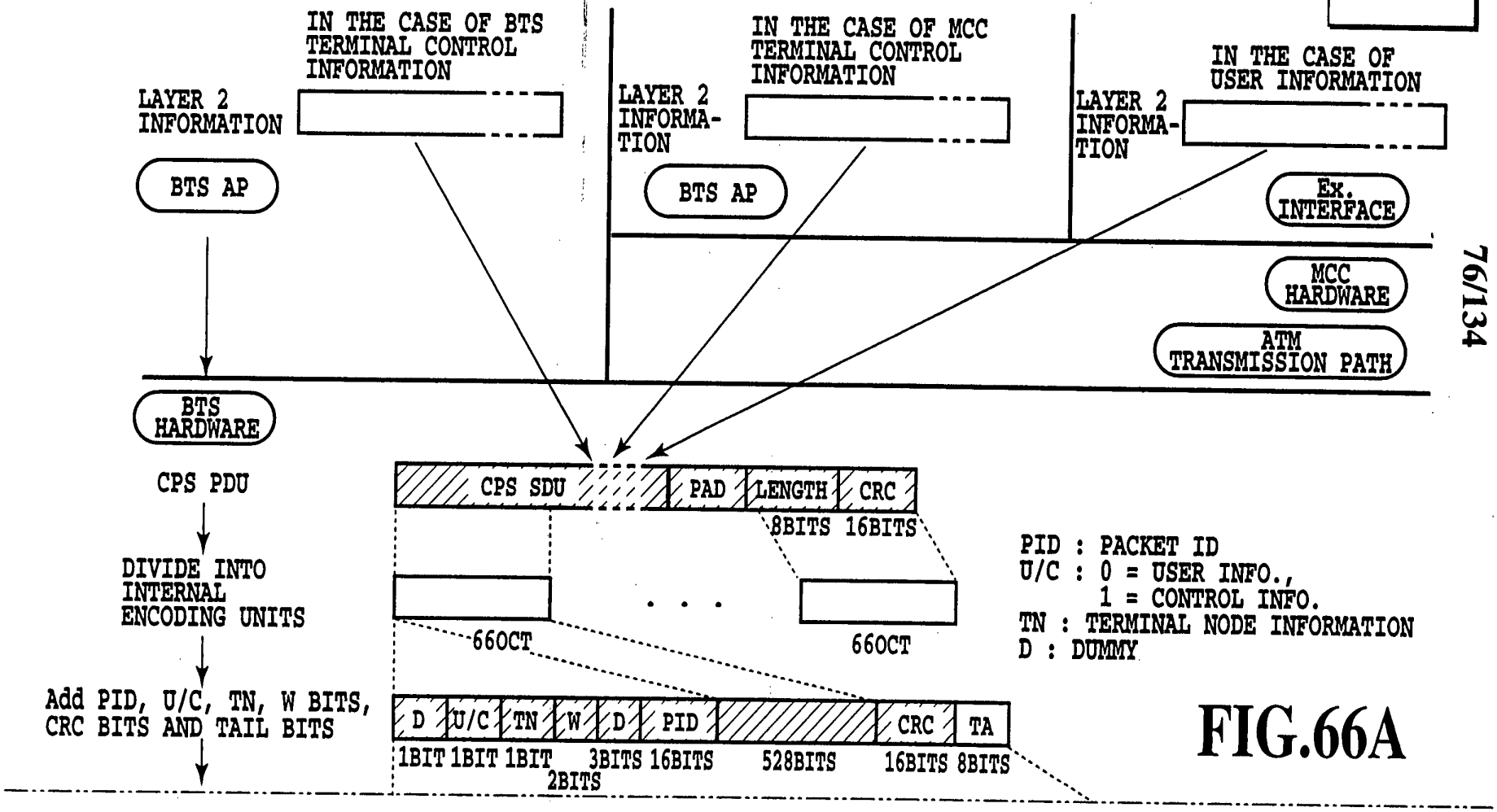


FIG.66A

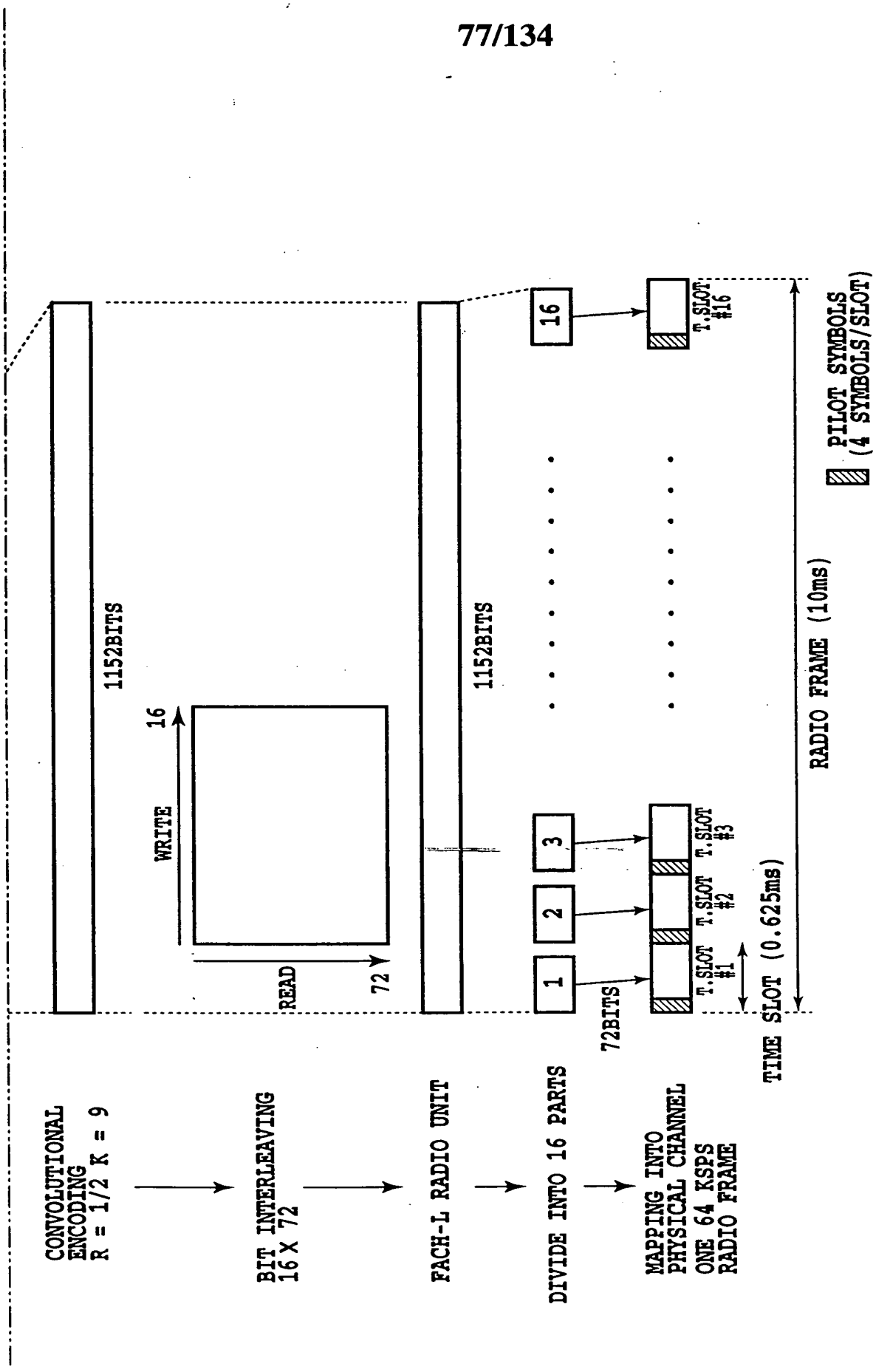

CONVOLUTIONAL ENCODING R = 1/2 K = 9
BIT INTERLEAVING 16 X 72
FACH-L RADIO UNIT
DIVIDE INTO 16 PARTS
MAPPING INTO PHYSICAL CHANNEL ONE 64 KSPS RADIO FRAME
1152BITS
16
WRITE
READ
72
1152BITS
1
2
3
16
72BITS
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS (4 SYMBOLS/SLOT)

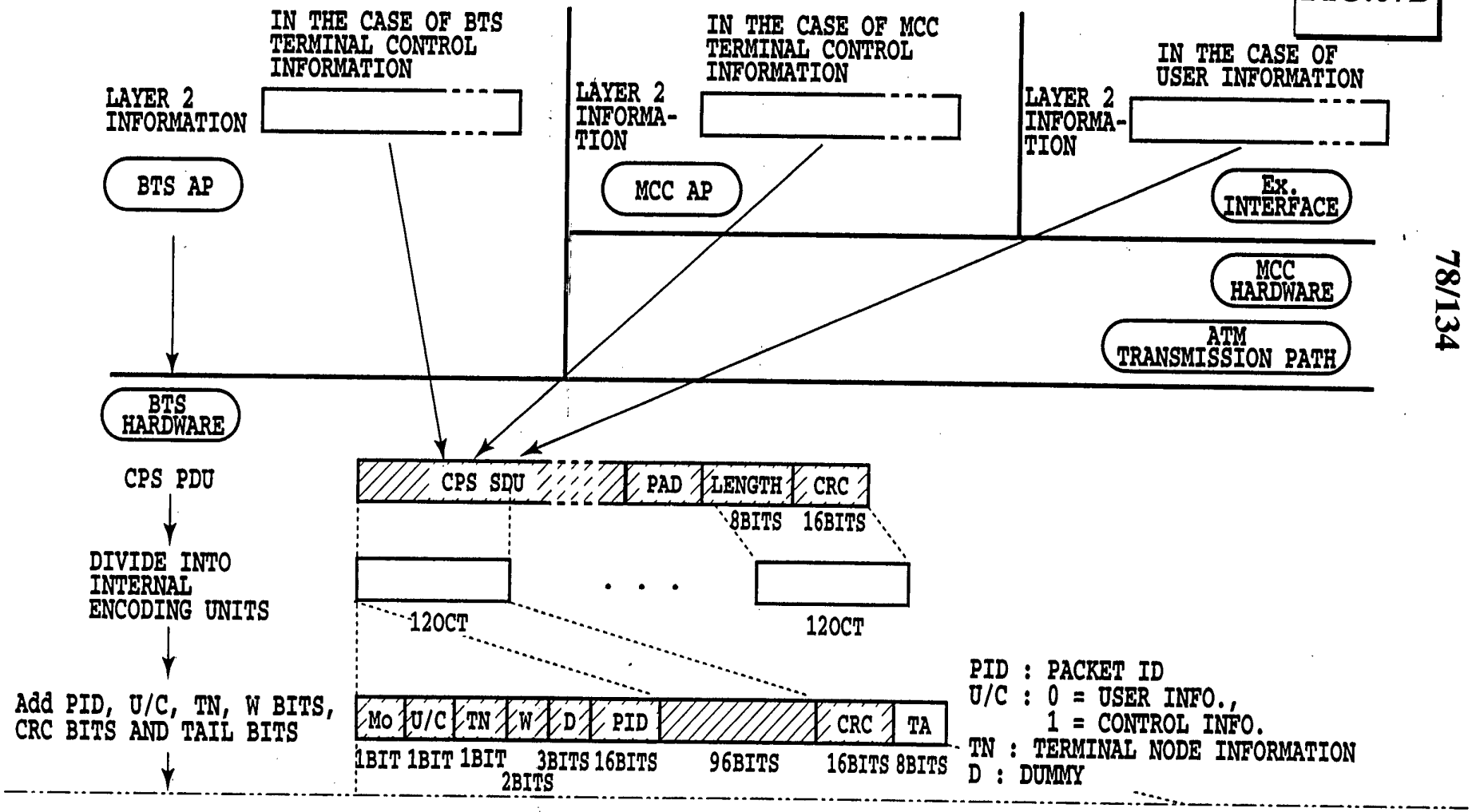
FIG.66B

FIG.67

FIG.67A

FIG.67B

FIG.67A



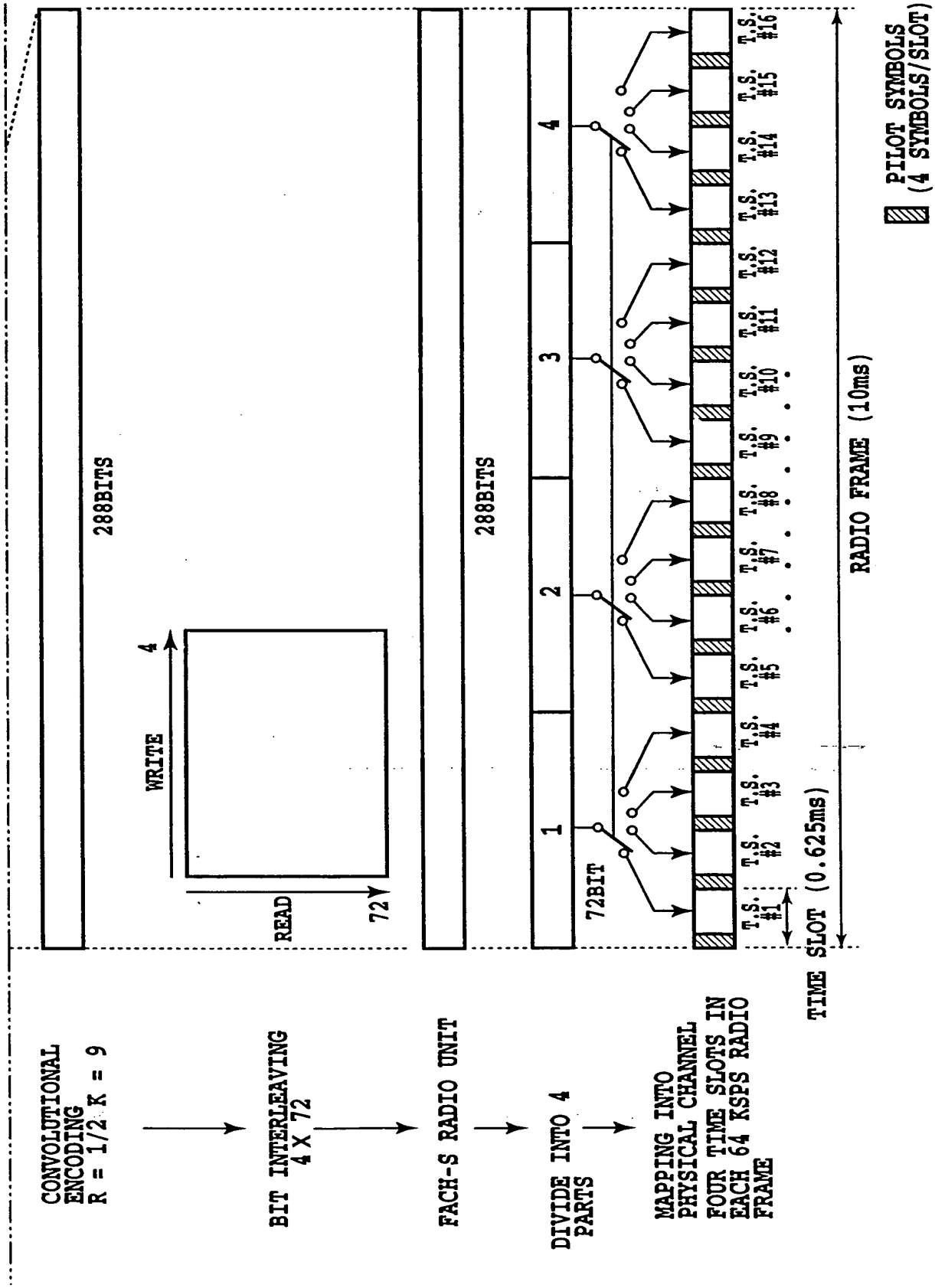

CONVOLUTIONAL ENCODING R = 1/2 K = 9
288BITS
BIT INTERLEAVING 4 X 72
WRITE
4
READ
72
FACH-S RADIO UNIT
288BITS
DIVIDE INTO 4 PARTS
1
2
3
4
72BIT
MAPPING INTO PHYSICAL CHANNEL FOUR TIME SLOTS IN EACH 64 KSPS RADIO FRAME
T.S. #1
T.S. #2
T.S. #3
T.S. #4
T.S. #5
T.S. #6
T.S. #7
T.S. #8
T.S. #9
T.S. #10
T.S. #11
T.S. #12
T.S. #13
T.S. #14
T.S. #15
T.S. #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS (4 SYMBOLS/SLOT)

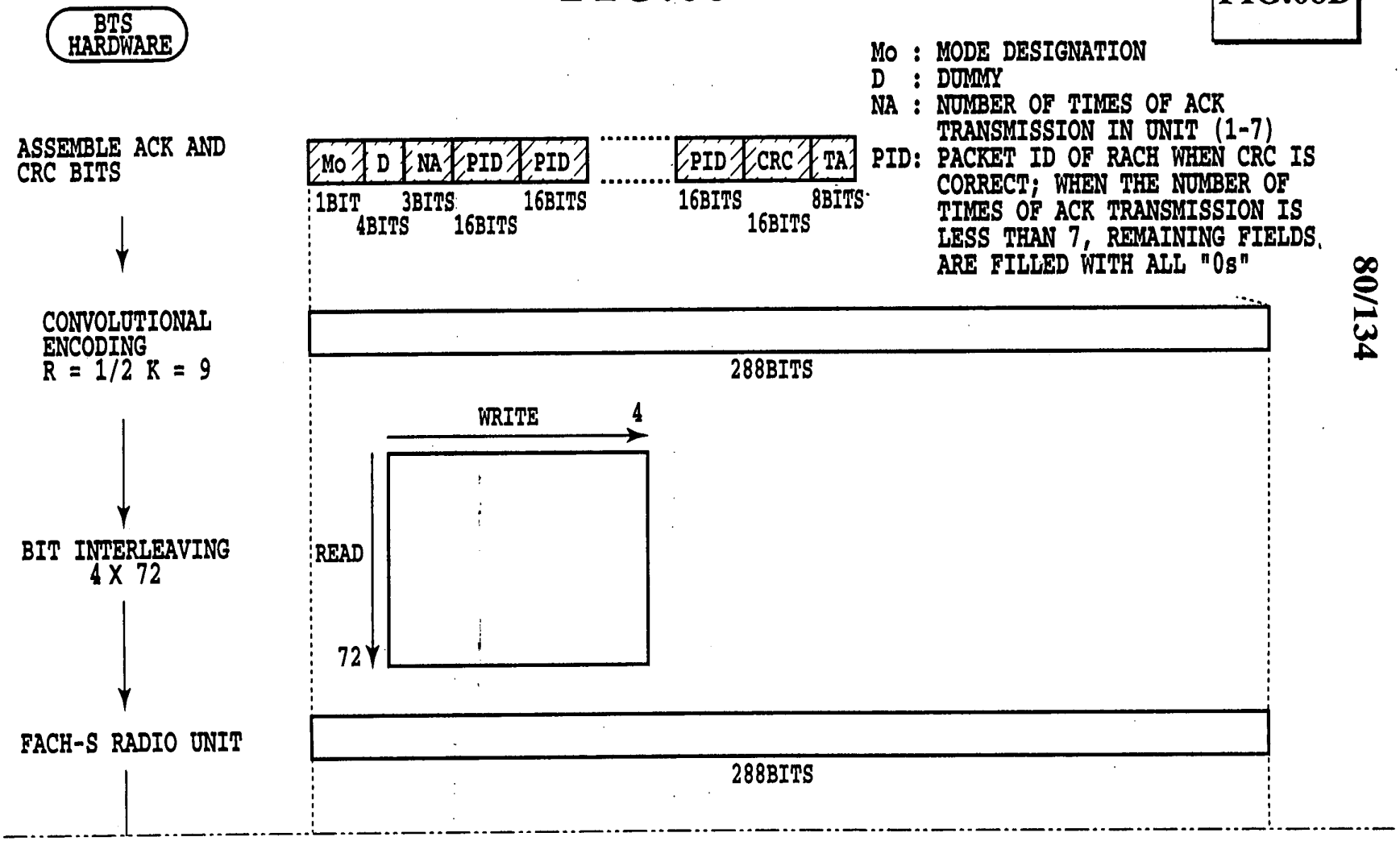
FIG.67B

FIG.68

FIG.68A

FIG.68B

FIG.68A



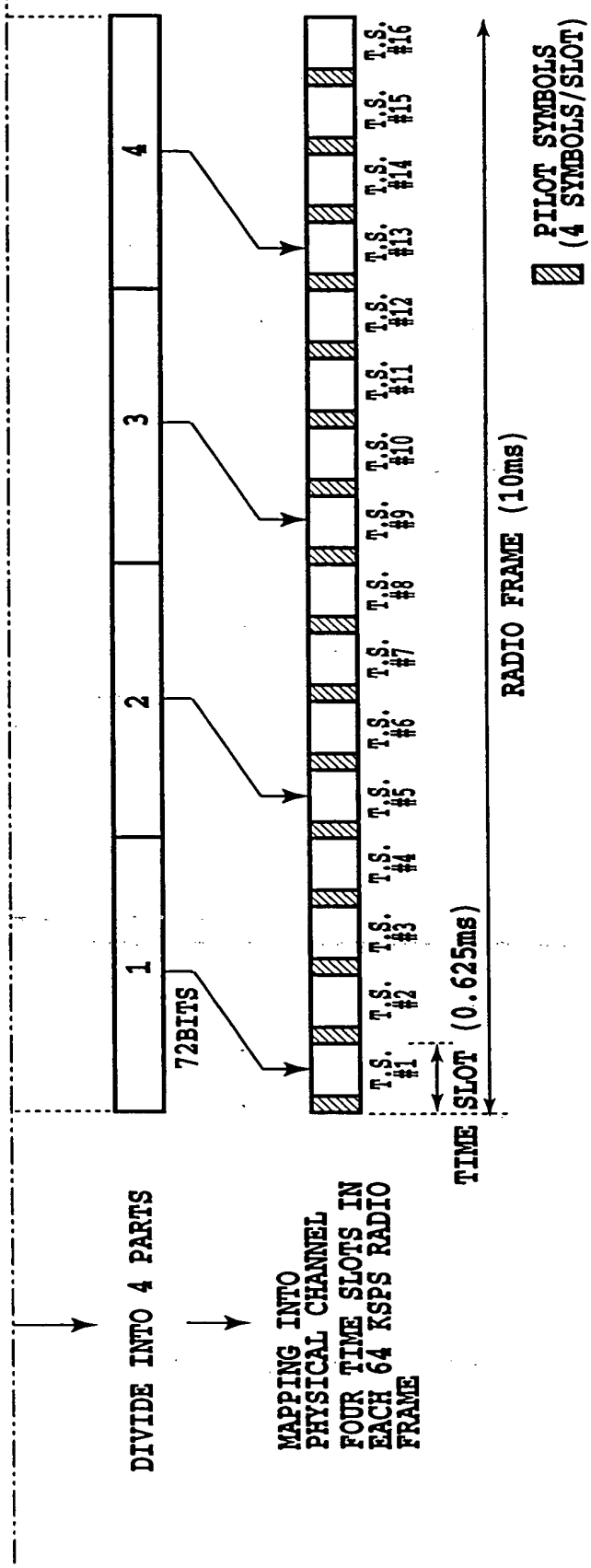

DIVIDE INTO 4 PARTS
MAPPING INTO PHYSICAL CHANNEL FOUR TIME SLOTS IN EACH 64 KSPS RADIO FRAME
1
2
3
4
72BITS
T.S. #1
T.S. #2
T.S. #3
T.S. #4
T.S. #5
T.S. #6
T.S. #7
T.S. #8
T.S. #9
T.S. #10
T.S. #11
T.S. #12
T.S. #13
T.S. #14
T.S. #15
T.S. #16
SLOT (0.625ms)
TIME
RADIO FRAME (10ms)
PILOT SYMBOLS (4 SYMBOLS/SLOT)

FIG.68B

FIG.69

FIG.69A

FIG.69B

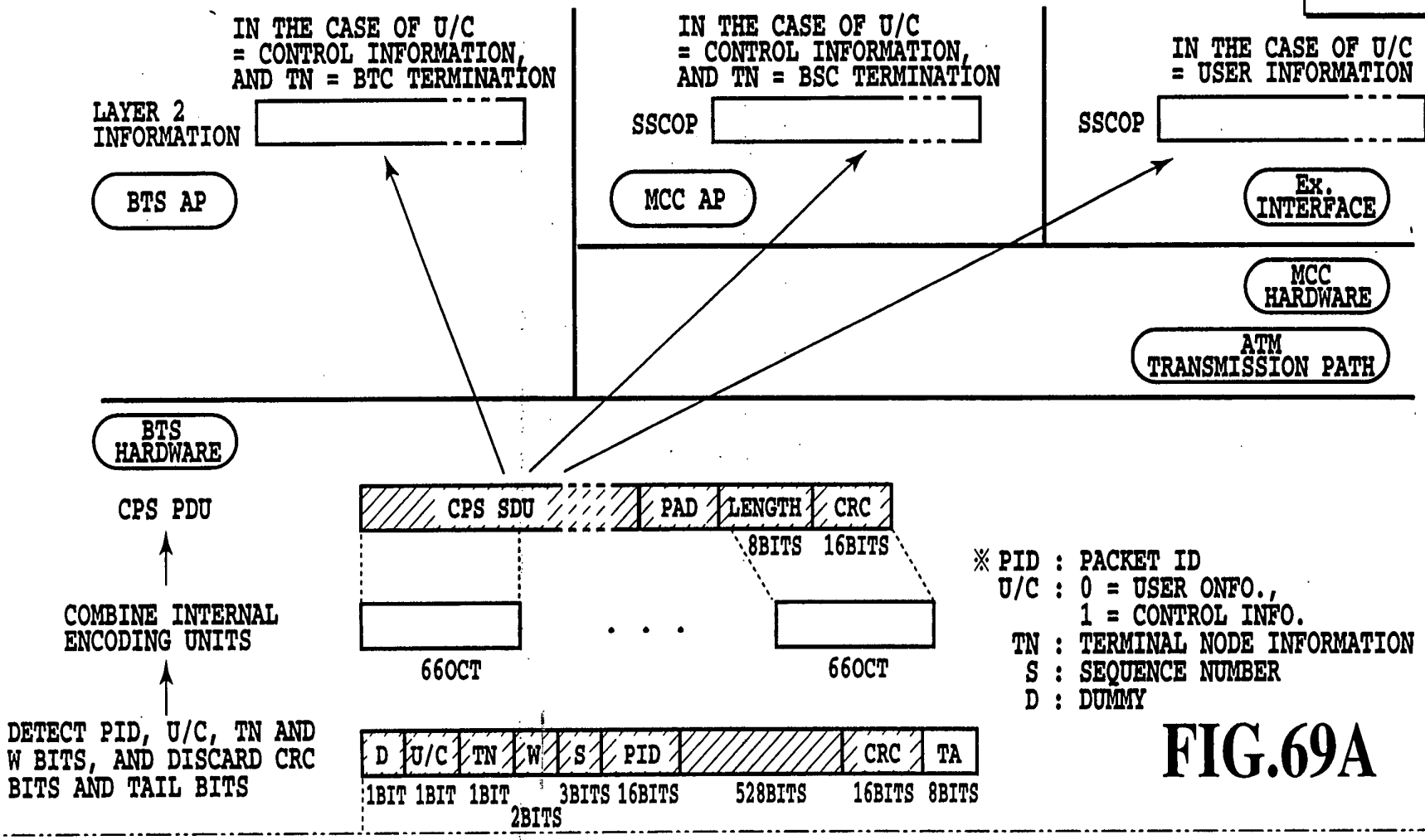


FIG.69A

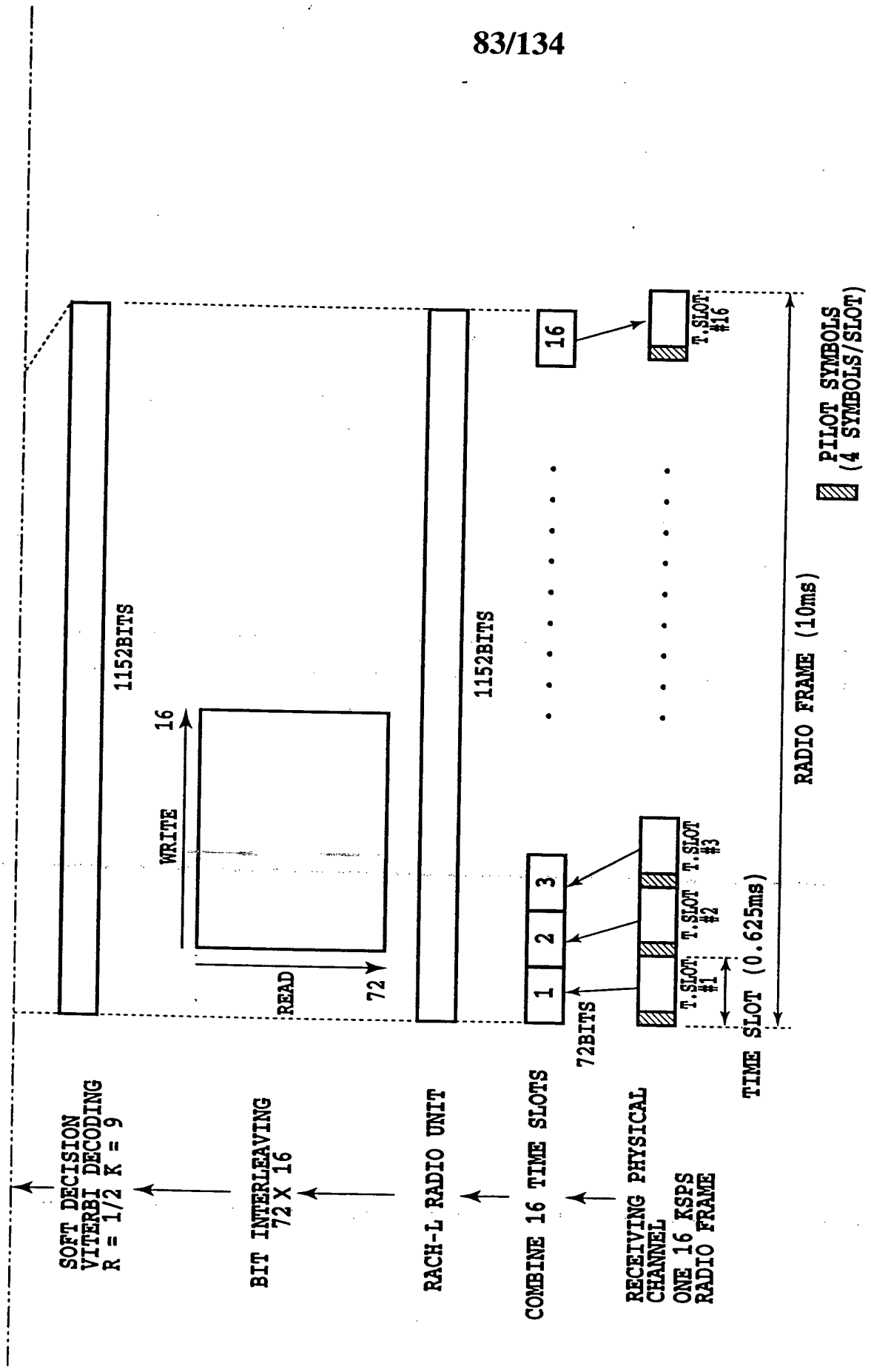

SOFT DECISION
VITERBI DECODING
R = 1/2 K = 9
BIT INTERLEAVING
72 X 16
RACH-L RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL
CHANNEL
ONE 16 KSPS
RADIO FRAME
1152BITS
WRITE
16
READ
72
1152BITS
1
2
3
16
72BITS
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS
(4 SYMBOLS/SLOT)

FIG.69B

FIG.70

FIG.70A

FIG.70B

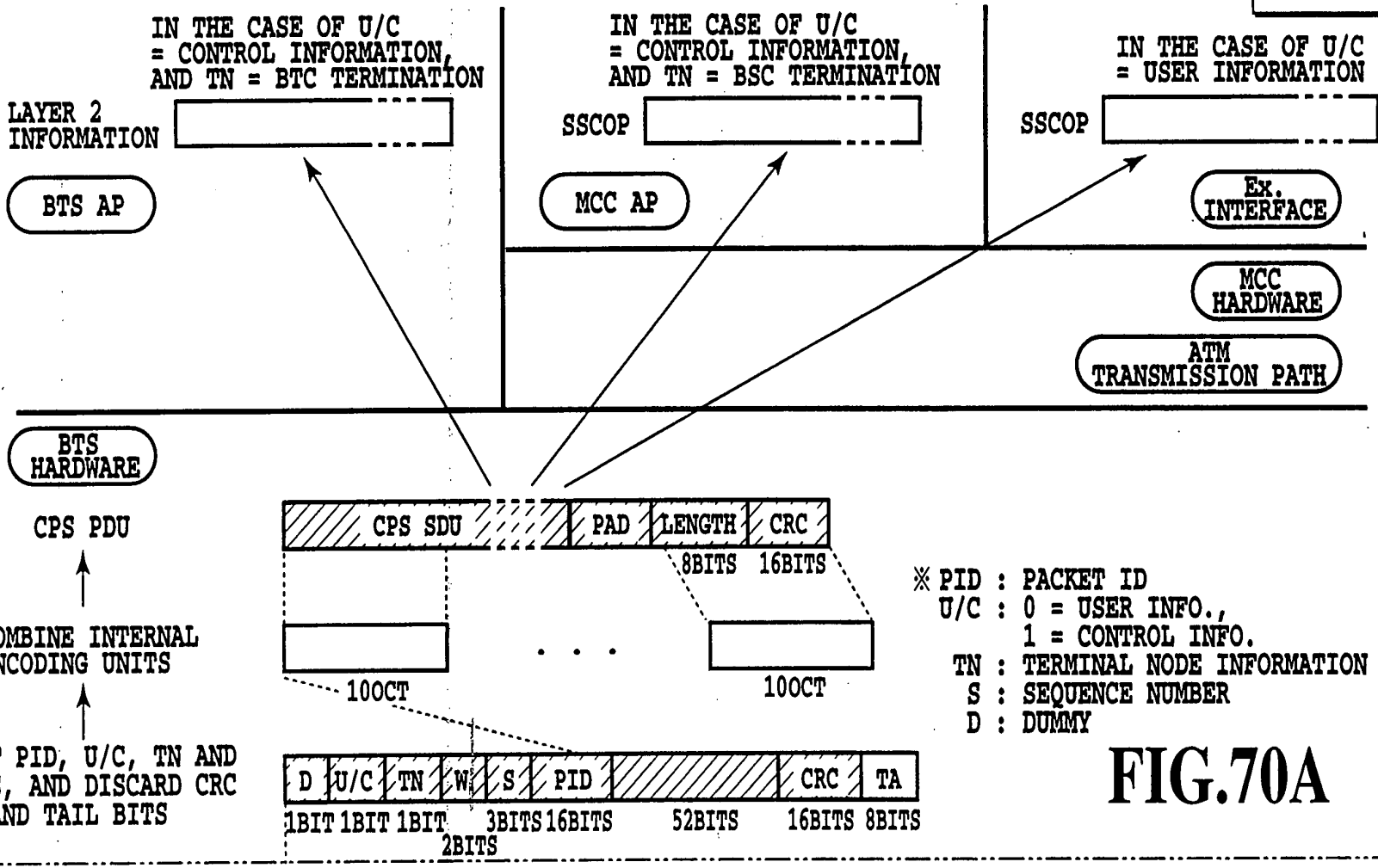


FIG.70A

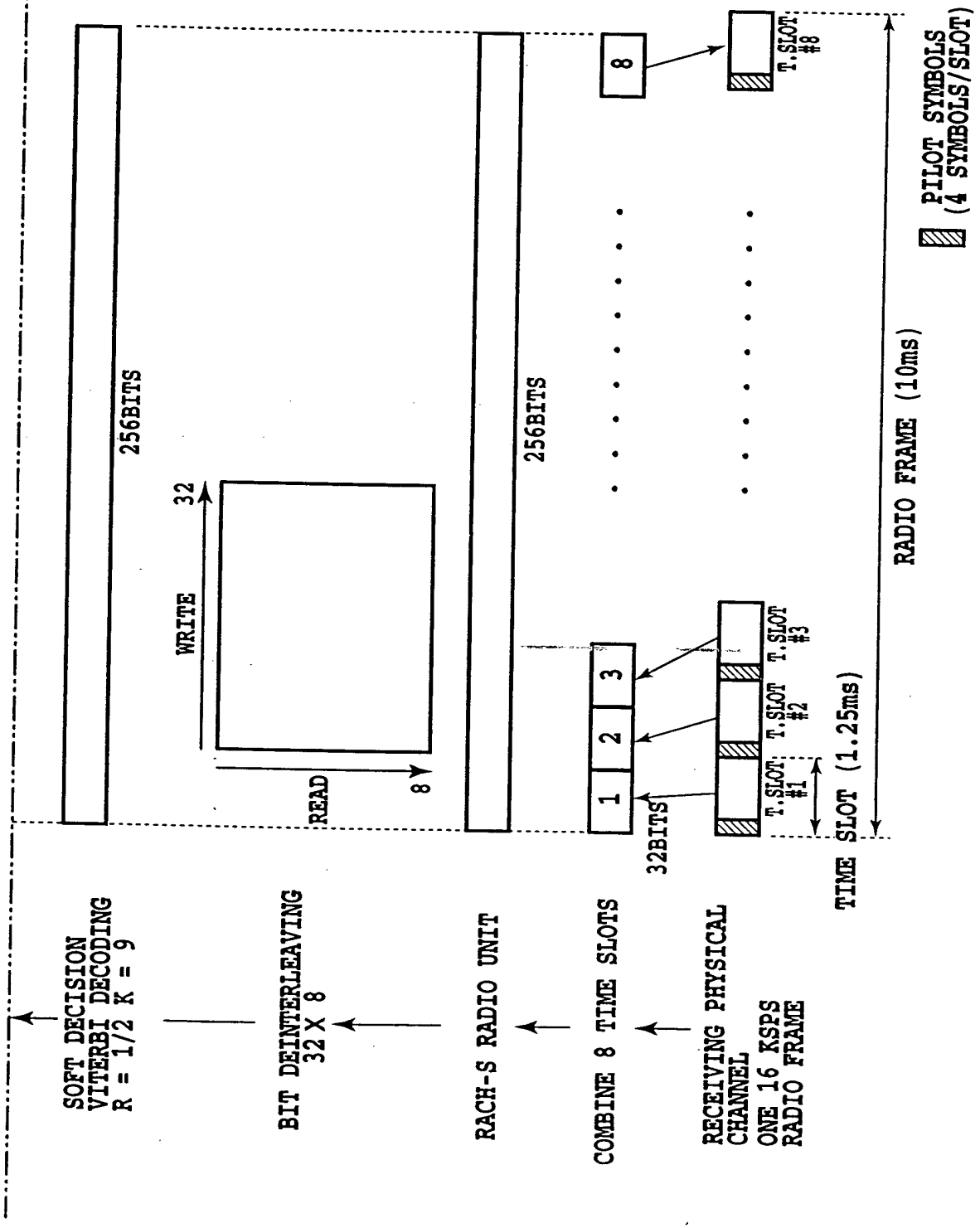

SOFT DECISION
VITERBI DECODING
R = 1/2 K = 9
BIT DEINTERLEAVING
32 X 8
RACH-S RADIO UNIT
COMBINE 8 TIME SLOTS
RECEIVING PHYSICAL
CHANNEL
ONE 16 KSPS
RADIO FRAME
256BITS
WRITE
32
READ
8
256BITS
1
2
3
8
32BITS
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #8
TIME SLOT (1.25ms)
RADIO FRAME (10ms)
PILOT SYMBOLS
(4 SYMBOLS/SLOT)

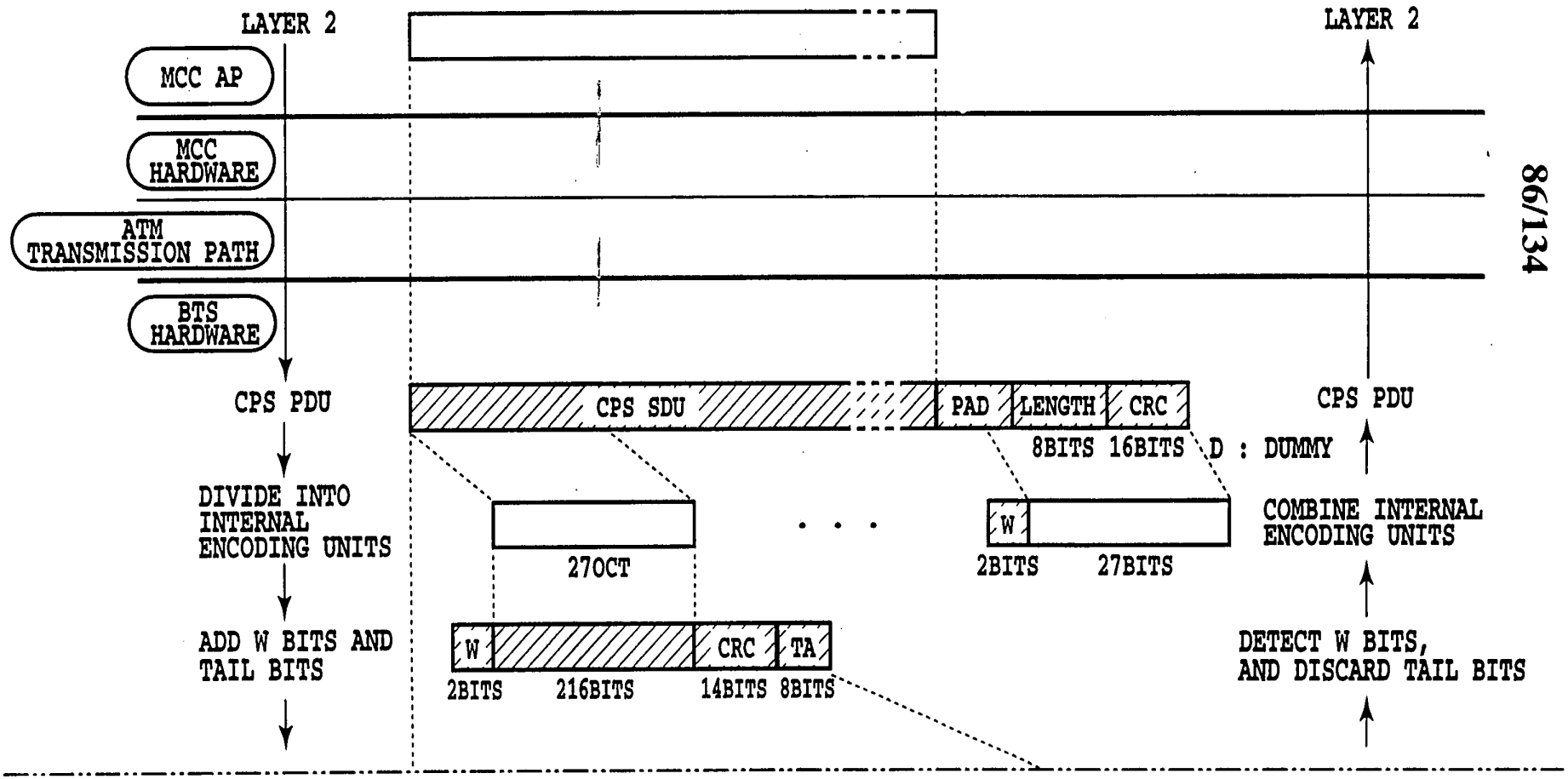
FIG.70B

FIG.71

FIG.71A

FIG.71B

FIG.71A



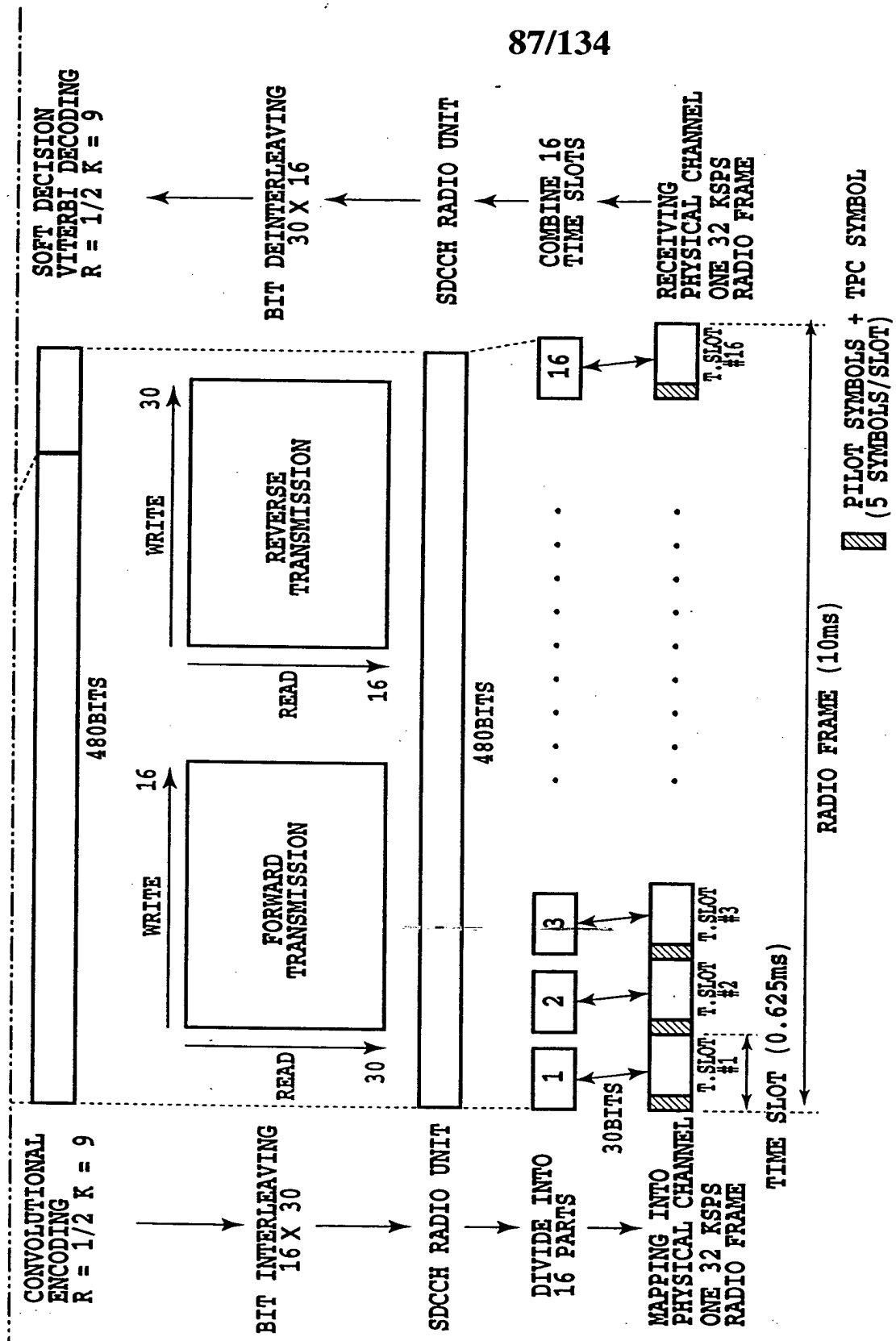

CONVOLUTIONAL ENCODING R = 1/2 K = 9
BIT INTERLEAVING 16 X 30
SDCCH RADIO UNIT
DIVIDE INTO 16 PARTS
MAPPING INTO PHYSICAL CHANNEL ONE 32 KSPS RADIO FRAME
480BITS
WRITE
16
FORWARD TRANSMISSION
READ
30
30BITS
1
2
3
T.SLOT #1
T.SLOT #2
T.SLOT #3
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
480BITS
WRITE
30
REVERSE TRANSMISSION
READ
16
16
T.SLOT #16
RECEIVING PHYSICAL CHANNEL ONE 32 KSPS RADIO FRAME
COMBINE 16 TIME SLOTS
SDCCH RADIO UNIT
BIT DEINTERLEAVING 30 X 16
SOFT DECISION VITERBI DECODING R = 1/2 K = 9
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)

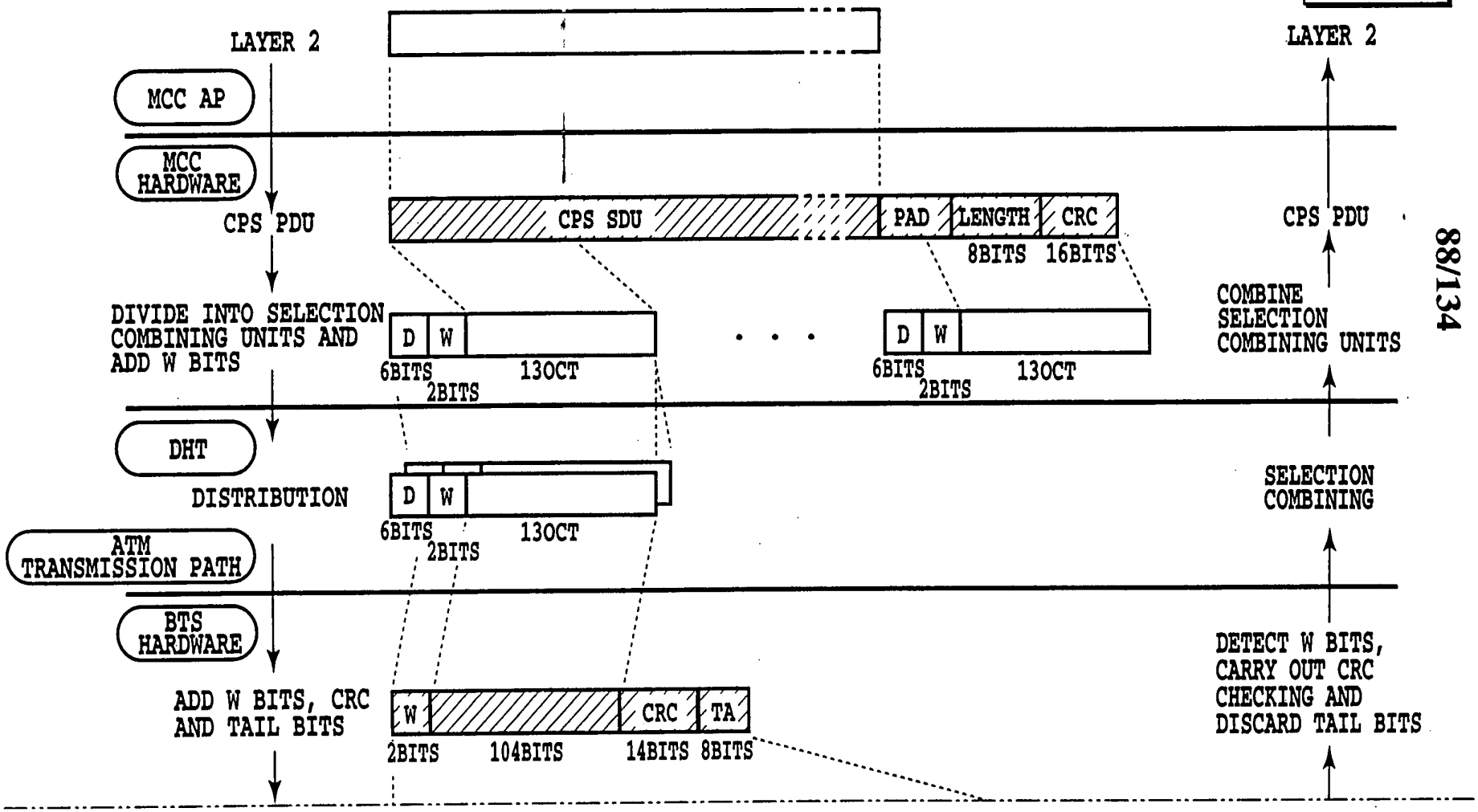
FIG.71B

FIG.72

FIG.72A

FIG.72B

FIG.72A



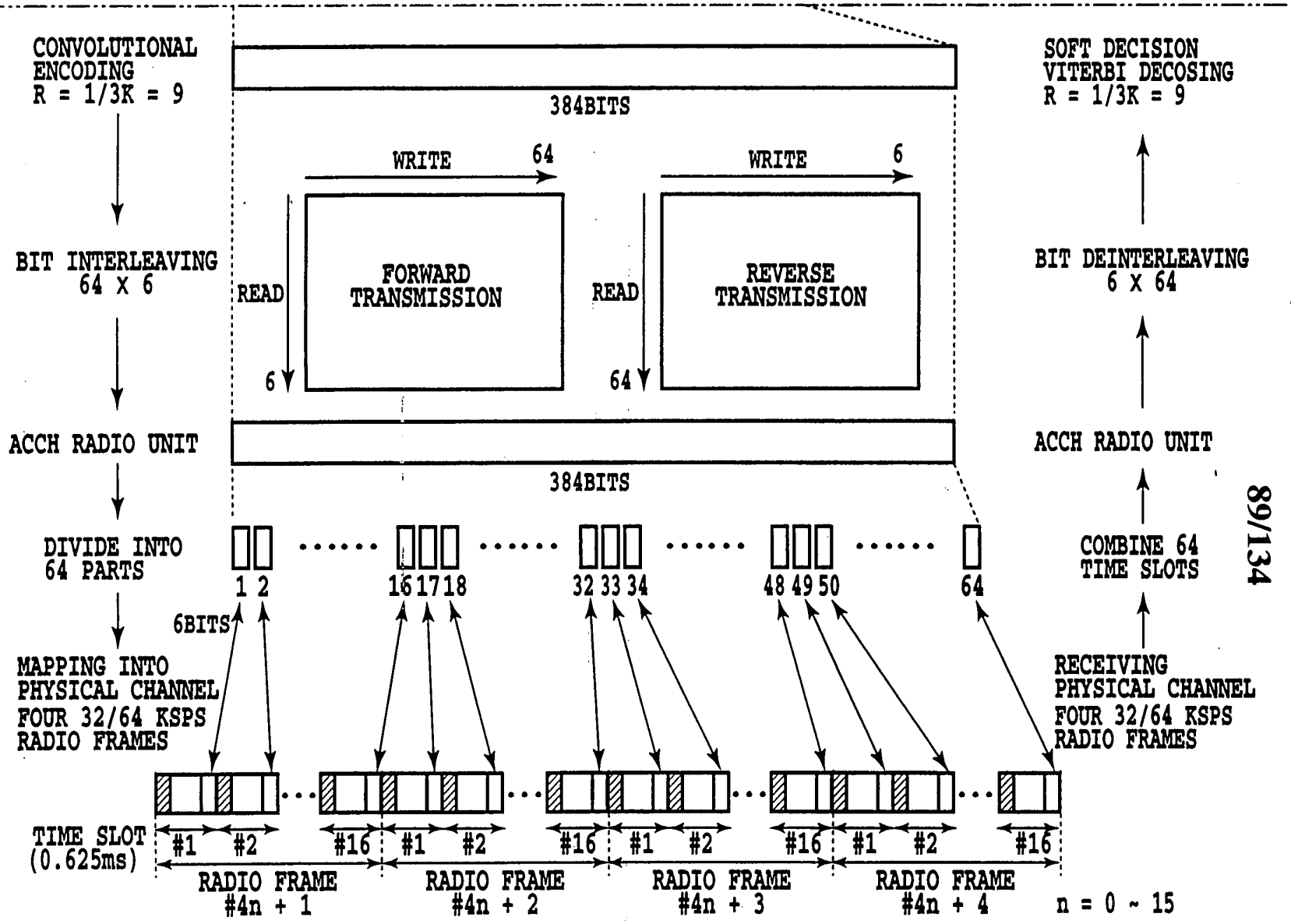

CONVOLUTIONAL ENCODING R = 1/3K = 9
BIT INTERLEAVING 64 X 6
ACCH RADIO UNIT
DIVIDE INTO 64 PARTS
6BITS
MAPPING INTO PHYSICAL CHANNEL FOUR 32/64 KSPS RADIO FRAMES
384BITS
WRITE
64
READ
6
FORWARD TRANSMISSION
WRITE
6
READ
64
REVERSE TRANSMISSION
384BITS
1 2
16 17 18
32 33 34
48 49 50
64
TIME SLOT (0.625ms)
#1 #2 #16 #1 #2 #16 #1 #2 #16 #1 #2 #16
RADIO FRAME #4n + 1
RADIO FRAME #4n + 2
RADIO FRAME #4n + 3
RADIO FRAME #4n + 4
n = 0 ~ 15
SOFT DECISION VITERBI DECOSING R = 1/3K = 9
BIT DEINTERLEAVING 6 X 64
ACCH RADIO UNIT
COMBINE 64 TIME SLOTS
RECEIVING PHYSICAL CHANNEL FOUR 32/64 KSPS RADIO FRAMES
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)

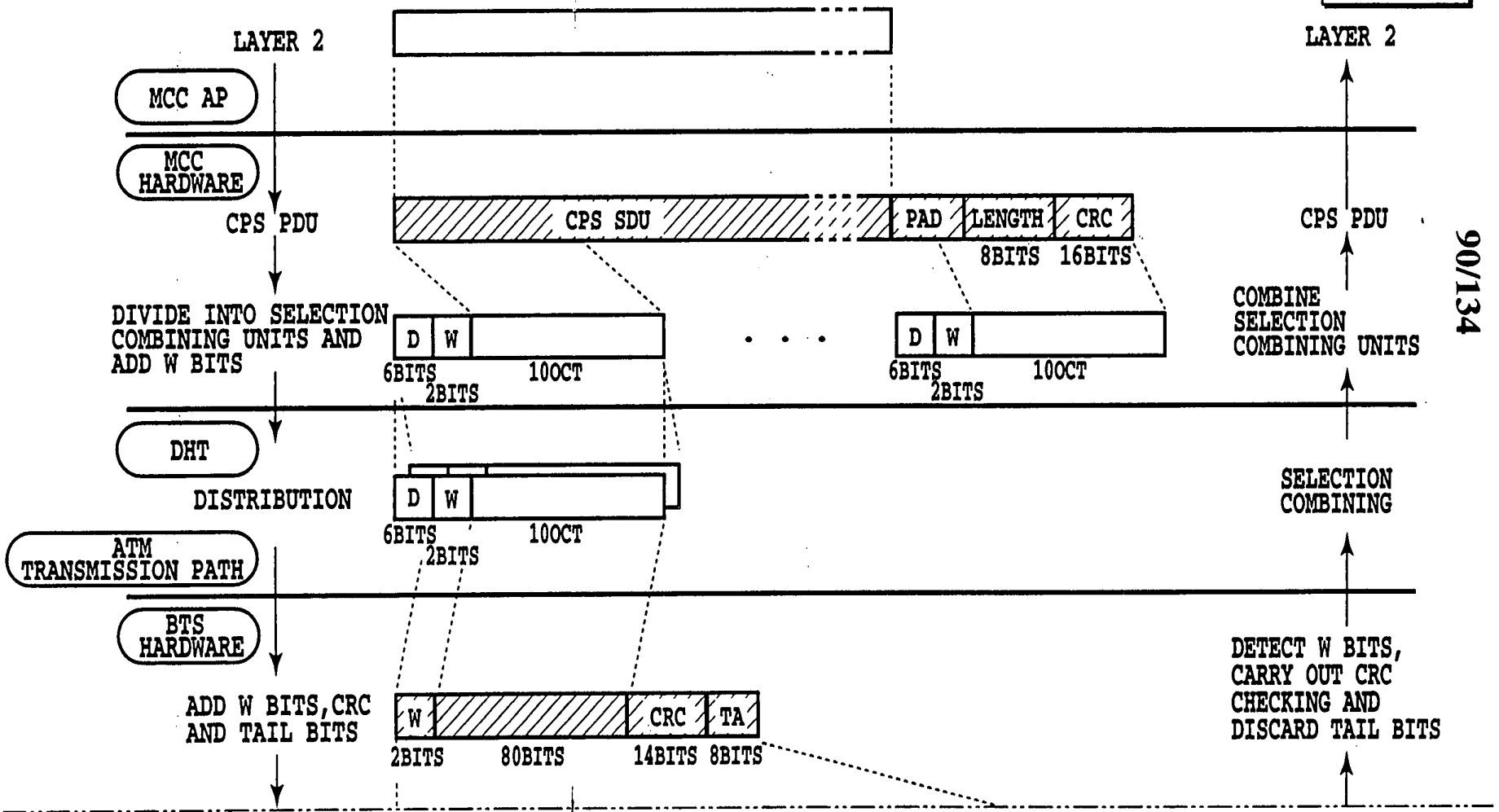
FIG.72B

FIG.73

FIG.73A

FIG.73B

FIG.73A



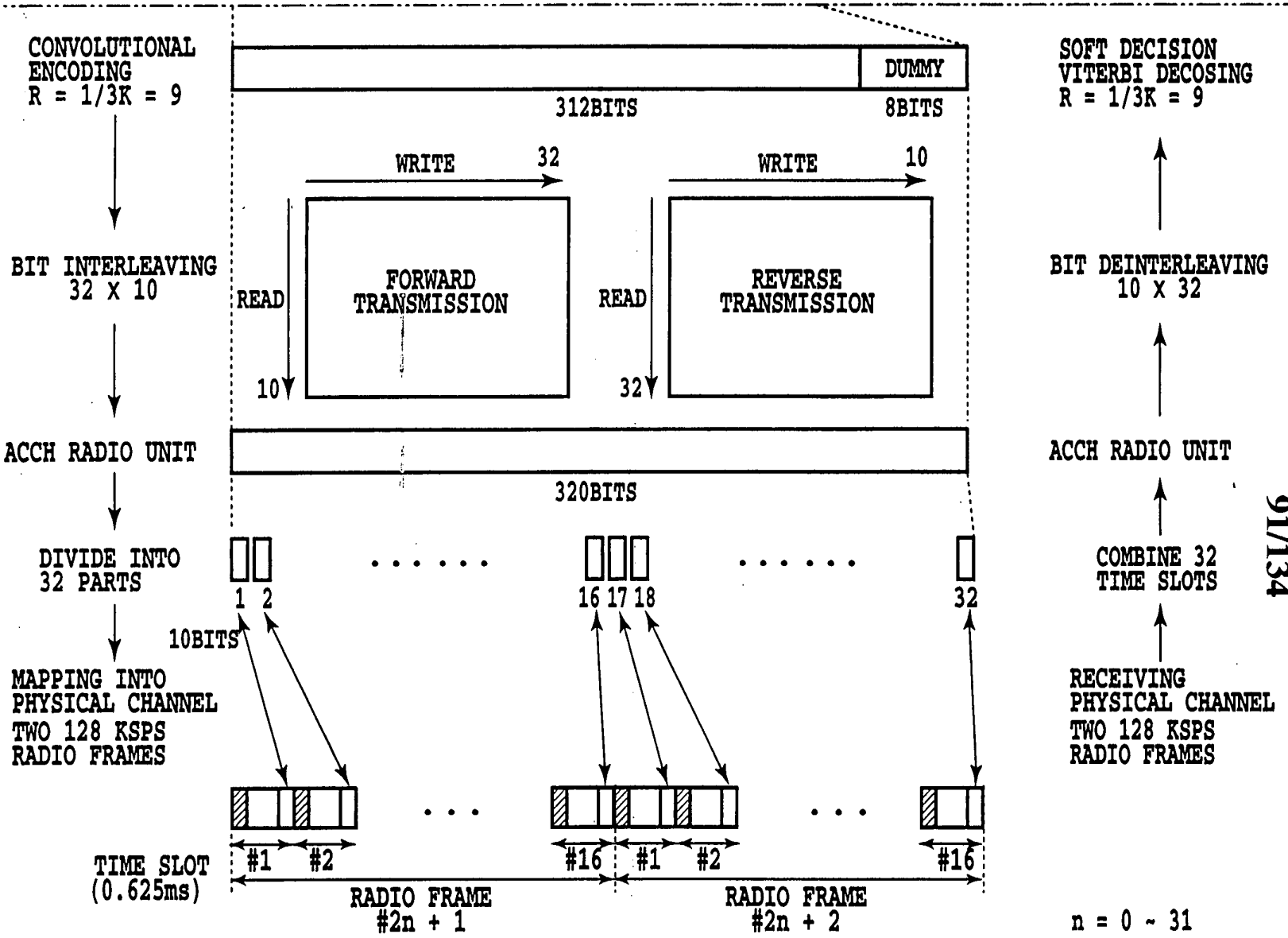

CONVOLUTIONAL ENCODING R = 1/3K = 9
BIT INTERLEAVING 32 X 10
ACCH RADIO UNIT
DIVIDE INTO 32 PARTS
10BITS
MAPPING INTO PHYSICAL CHANNEL TWO 128 KSPS RADIO FRAMES
TIME SLOT (0.625ms)
312BITS
DUMMY
8BITS
WRITE 32
WRITE 10
READ
10
FORWARD TRANSMISSION
READ
32
REVERSE TRANSMISSION
320BITS
1 2
16 17 18
32
#1 #2
#16 #1 #2
#16
RADIO FRAME #2n + 1
RADIO FRAME #2n + 2
SOFT DECISION VITERBI DECOSING R = 1/3K = 9
BIT DEINTERLEAVING 10 X 32
ACCH RADIO UNIT
COMBINE 32 TIME SLOTS
RECEIVING PHYSICAL CHANNEL TWO 128 KSPS RADIO FRAMES
n = 0 ~ 31
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)

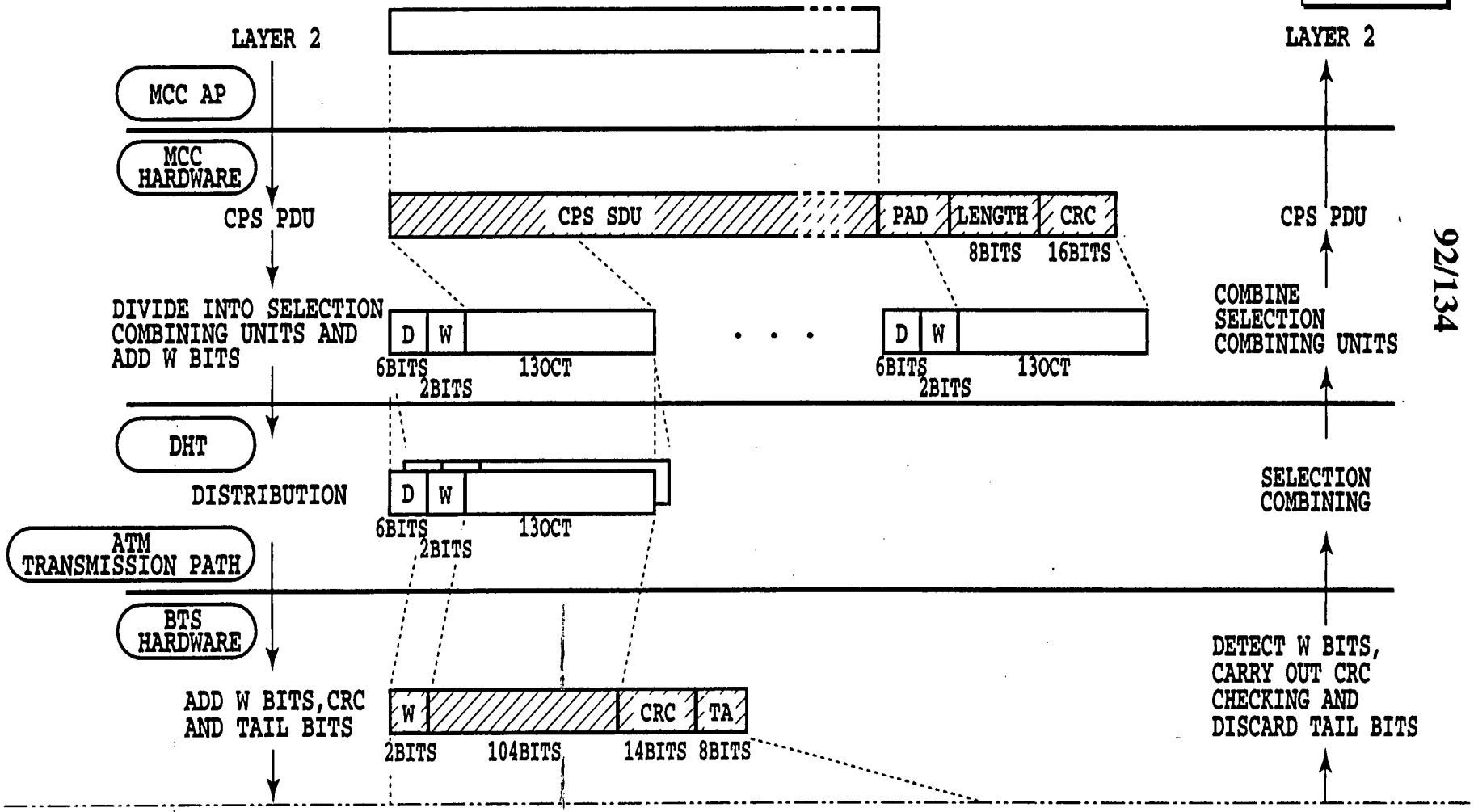
FIG.73B

FIG.74

FIG.74A

FIG.74B

FIG.74A



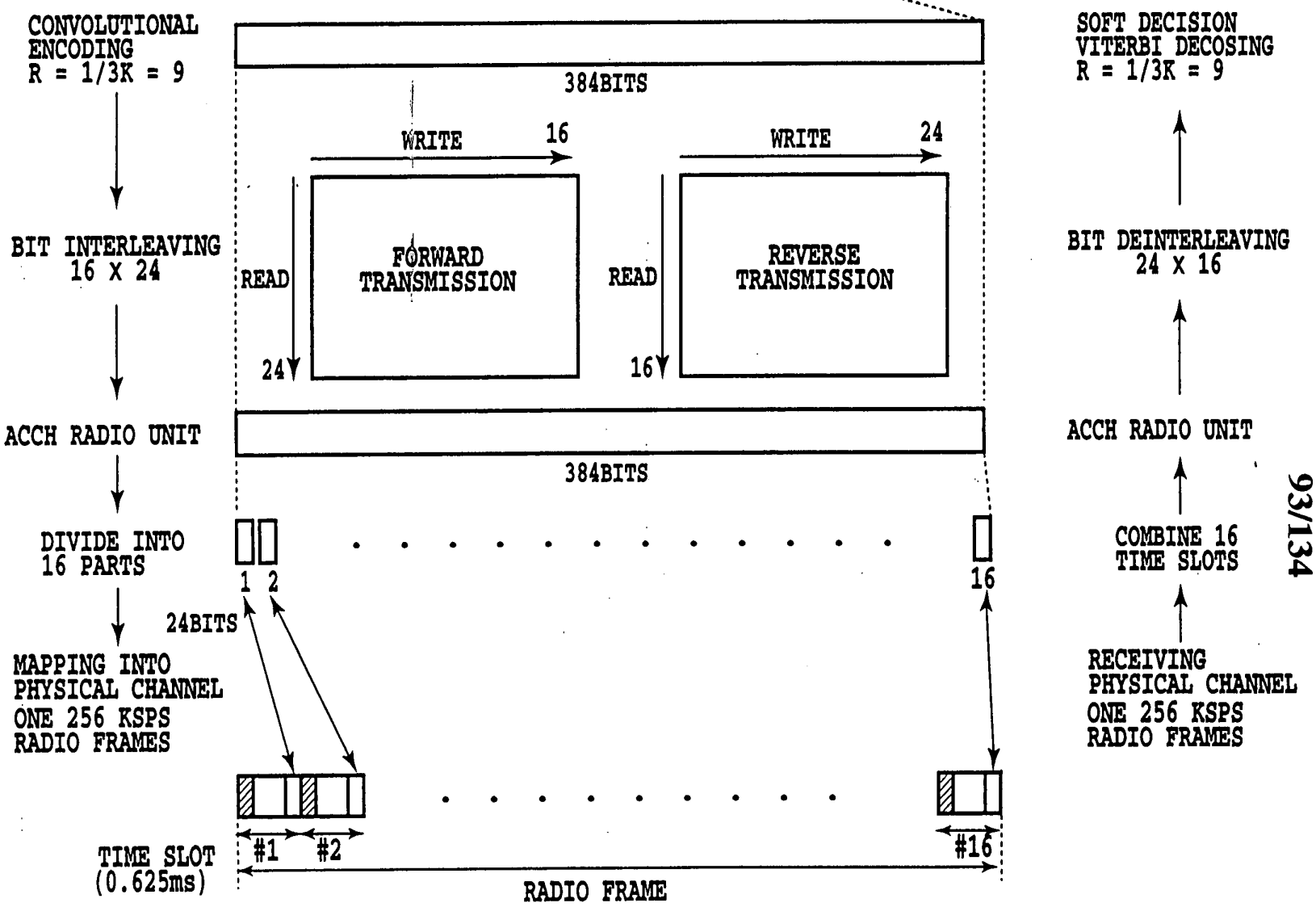

CONVOLUTIONAL ENCODING R = 1/3K = 9
BIT INTERLEAVING 16 X 24
ACCH RADIO UNIT
DIVIDE INTO 16 PARTS
24BITS
MAPPING INTO PHYSICAL CHANNEL ONE 256 KSPS RADIO FRAMES
384BITS
WRITE
16
WRITE
24
READ
24
FORWARD TRANSMISSION
READ
16
REVERSE TRANSMISSION
384BITS
1
2
16
#1
#2
#16
TIME SLOT (0.625ms)
RADIO FRAME
SOFT DECISION VITERBI DECOSING R = 1/3K = 9
BIT DEINTERLEAVING 24 X 16
ACCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 256 KSPS RADIO FRAMES
PILOT SYMBOLS + TPC SYMBOL (9 SYMBOLS/SLOT)

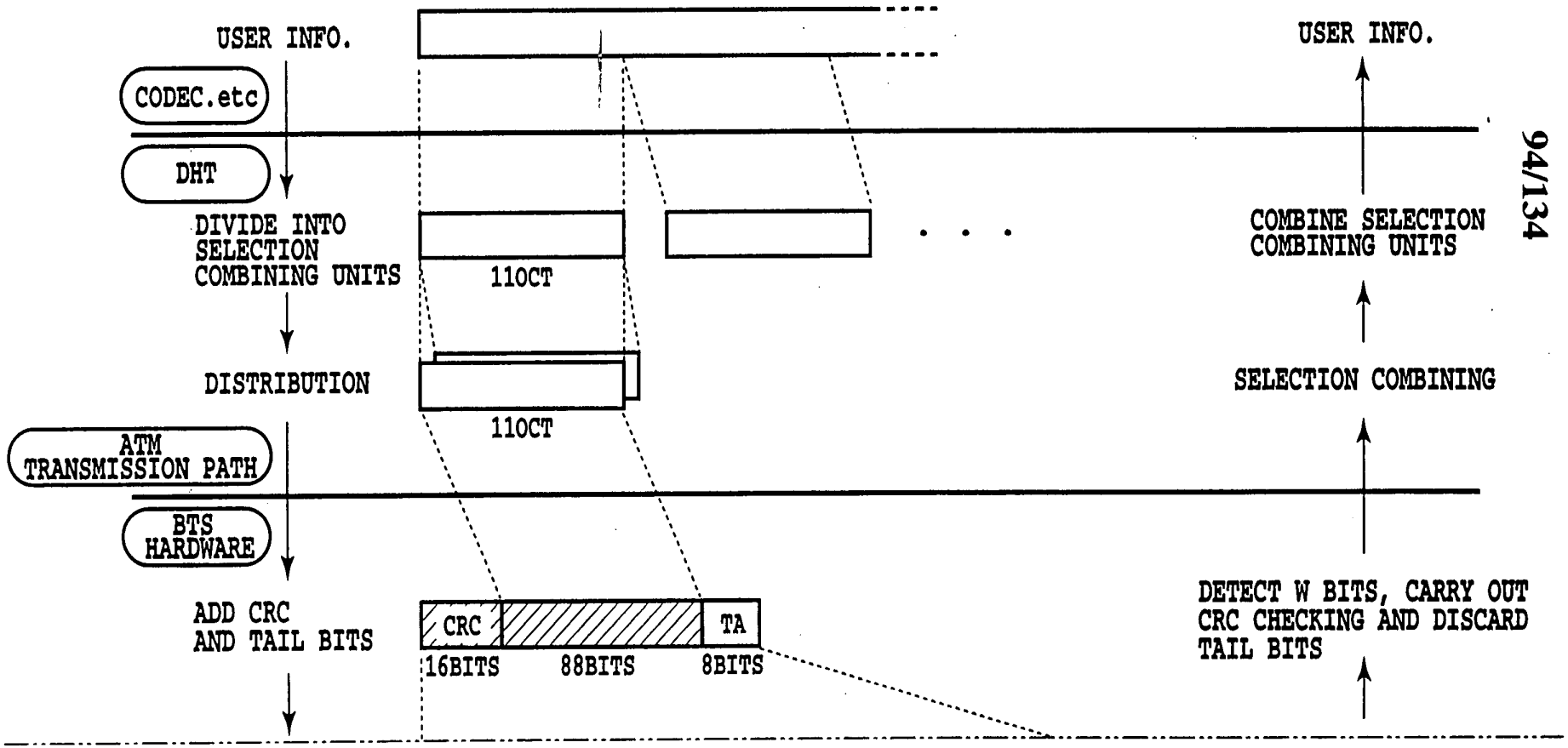
FIG.74B

FIG.75

FIG.75A

FIG.75B

FIG.75A



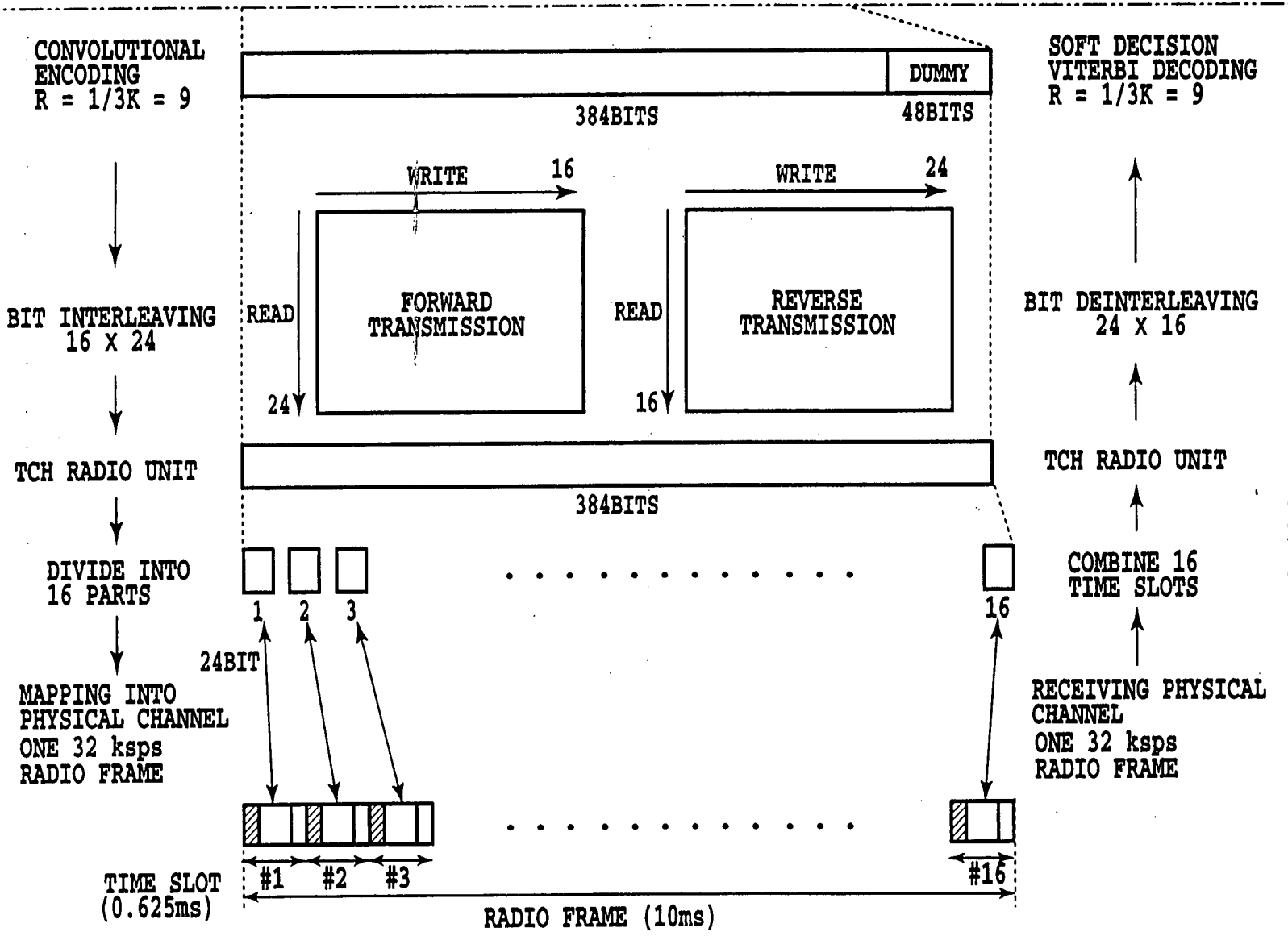

CONVOLUTIONAL ENCODING R = 1/3K = 9
BIT INTERLEAVING 16 X 24
TCH RADIO UNIT
DIVIDE INTO 16 PARTS
MAPPING INTO PHYSICAL CHANNEL ONE 32 ksps RADIO FRAME
384BITS
DUMMY
48BITS
WRITE
16
WRITE
24
READ
24
FORWARD TRANSMISSION
READ
16
REVERSE TRANSMISSION
384BITS
1
2
3
16
24BIT
#1
#2
#3
#16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
SOFT DECISION VITERBI DECODING R = 1/3K = 9
BIT DEINTERLEAVING 24 X 16
TCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 32 ksps RADIO FRAME
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)

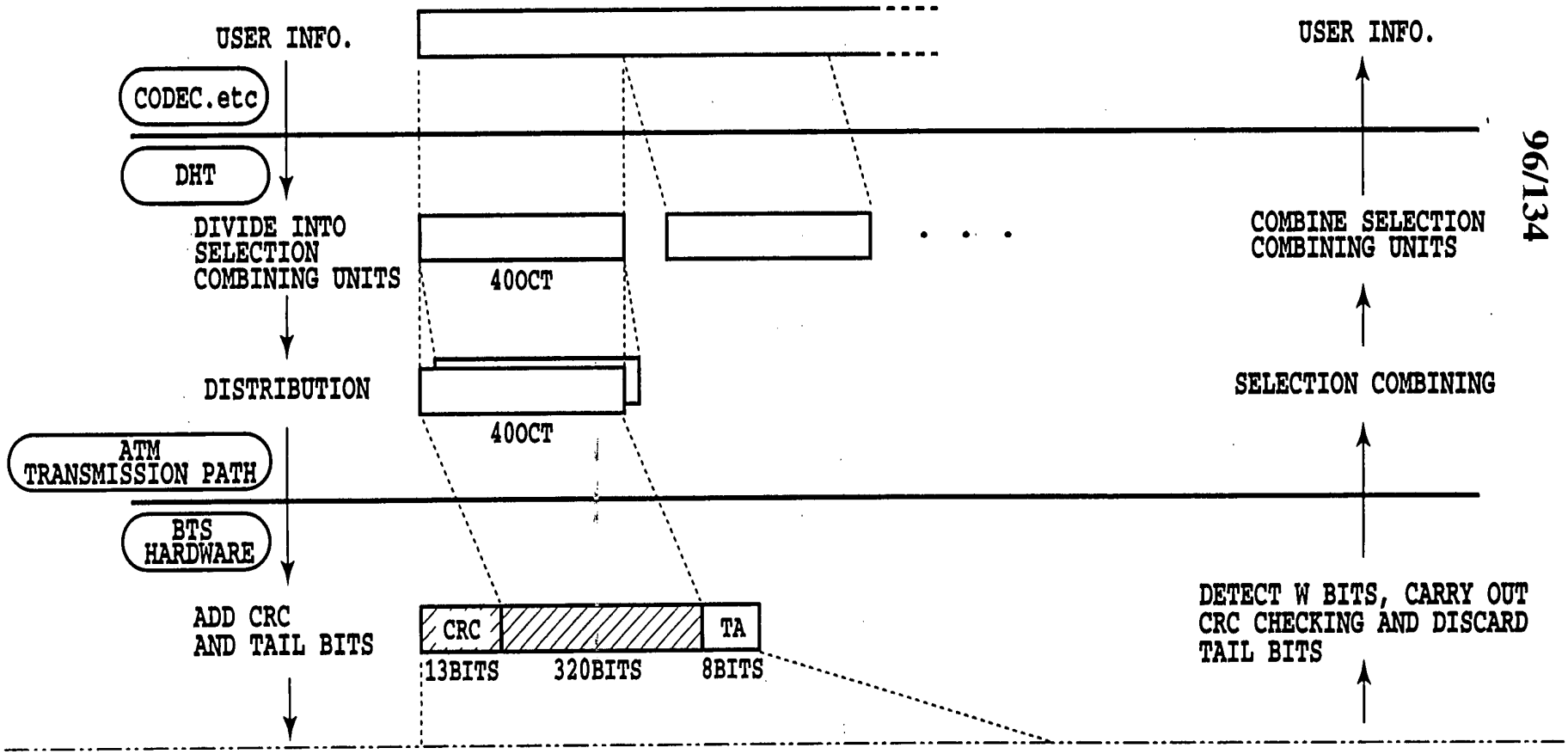
FIG.75B

FIG.76

FIG.76A

FIG.76B

FIG.76A



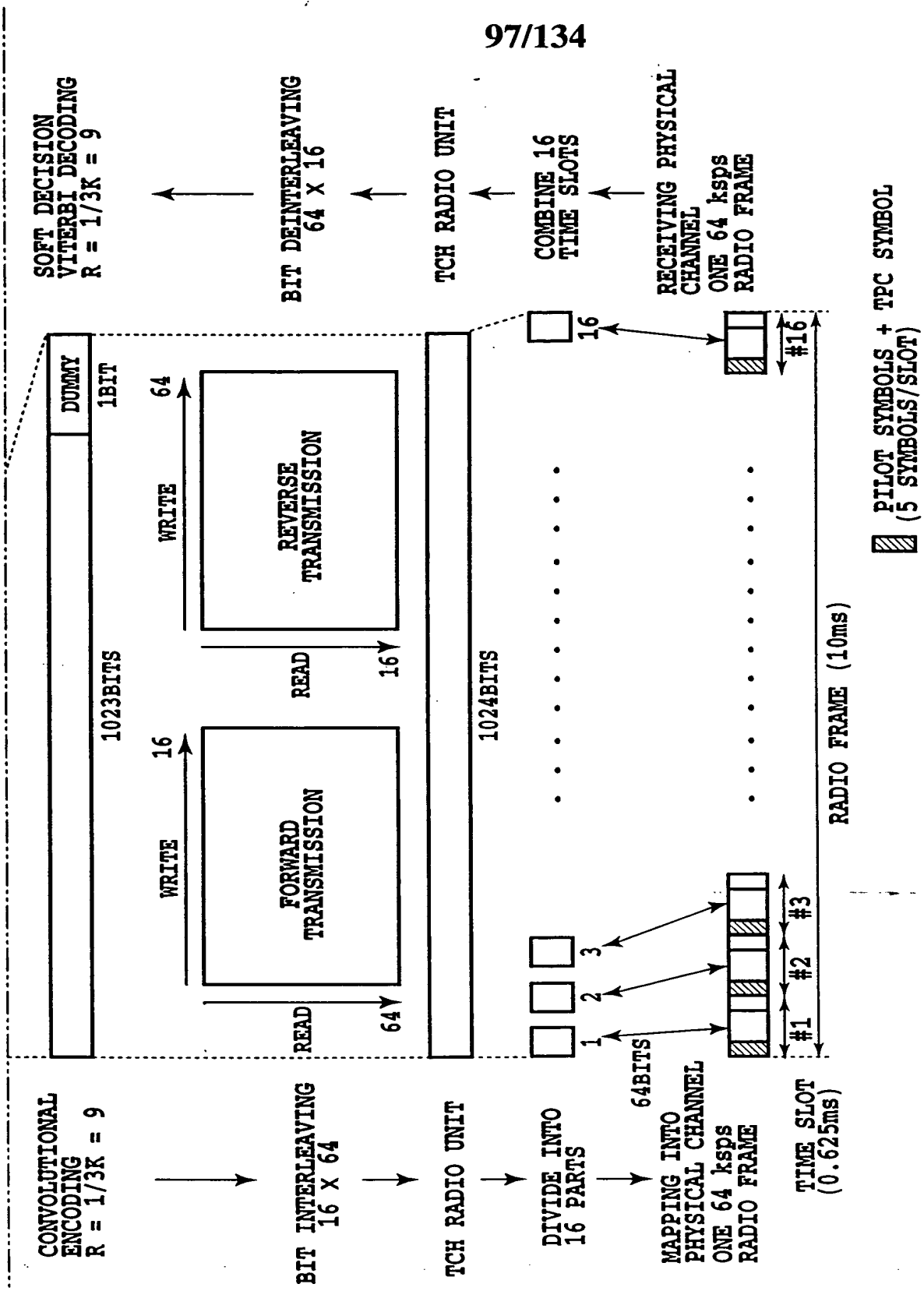
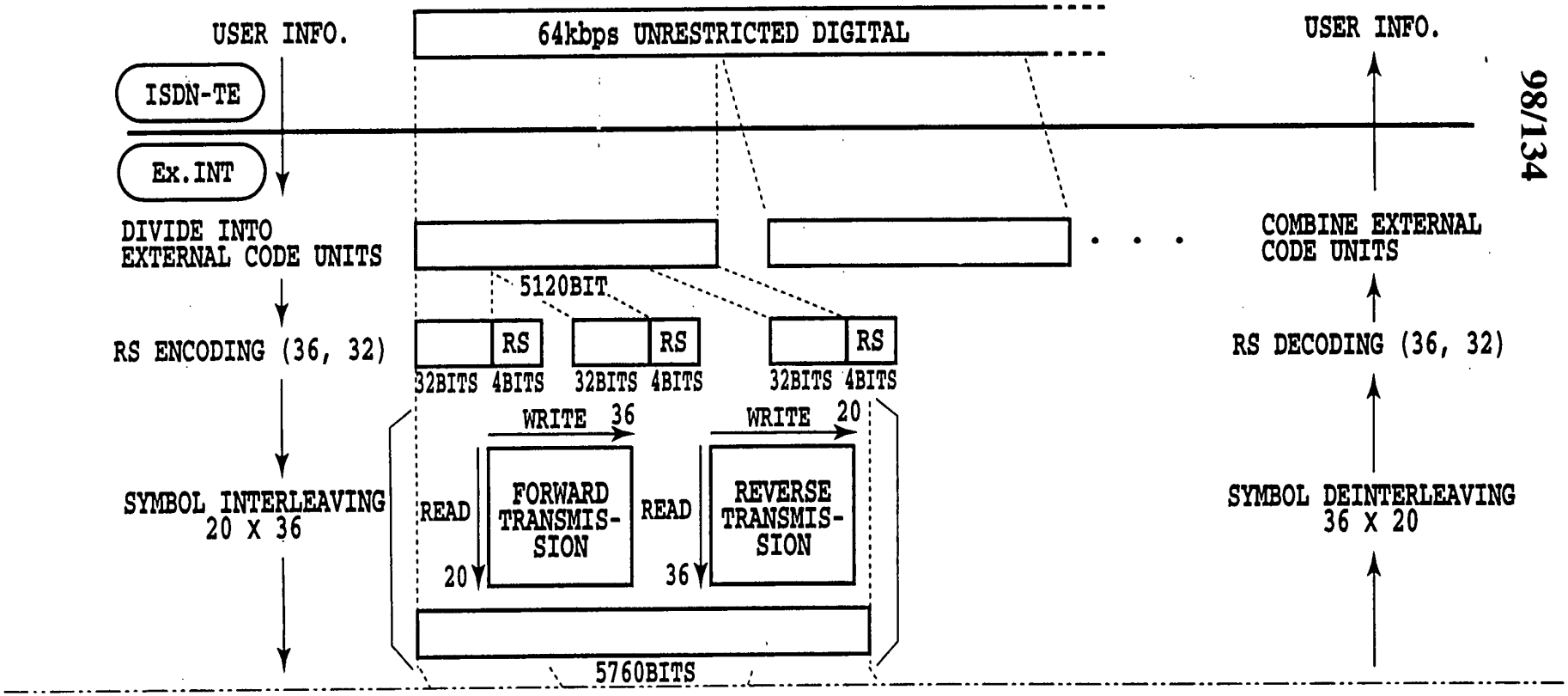

CONVOLUTIONAL ENCODING R = 1/3K = 9
BIT INTERLEAVING 16 X 64
TCH RADIO UNIT
DIVIDE INTO 16 PARTS
MAPPING INTO PHYSICAL CHANNEL ONE 64 ksps RADIO FRAME
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
1023BITS
DUMMY
1BIT
WRITE
16
64
FORWARD TRANSMISSION
REVERSE TRANSMISSION
READ
64
16
1024BITS
64BITS
1
2
3
#1
#2
#3
#16
16
COMBINE 16 TIME SLOTS
TCH RADIO UNIT
BIT DEINTERLEAVING 64 X 16
SOFT DECISION VITERBI DECODING R = 1/3K = 9
RECEIVING PHYSICAL CHANNEL ONE 64 ksps RADIO FRAME
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)

FIG.76B

FIG.77

FIG.77A
FIG.77B
FIG.77C

FIG.77A



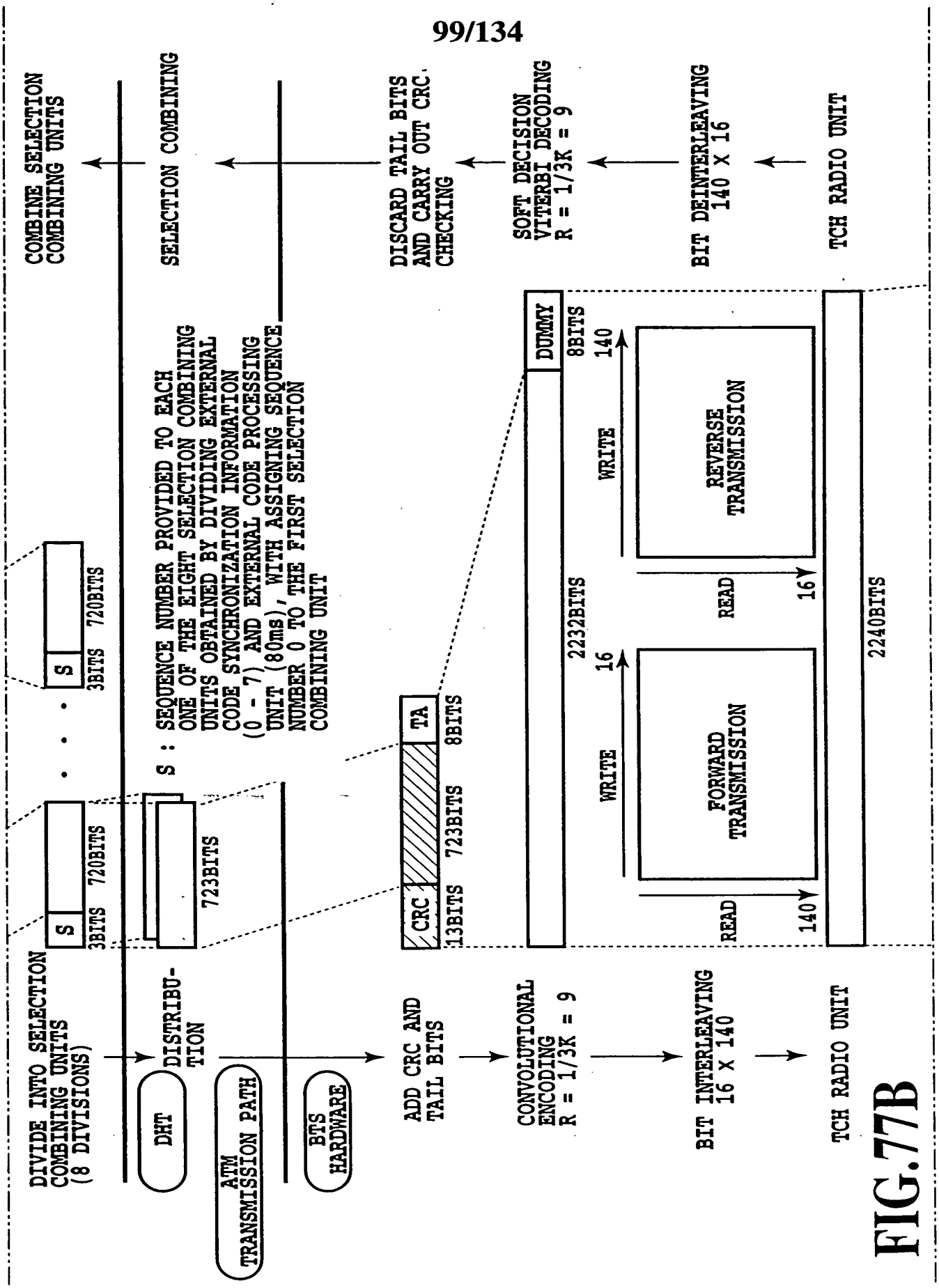

DIVIDE INTO SELECTION COMBINING UNITS (8 DIVISIONS)
DHT
DISTRIBU-TION
ATM TRANSMISSION PATH
BTS HARDWARE
ADD CRC AND TAIL BITS
CONVOLUTIONAL ENCODING R = 1/3K = 9
BIT INTERLEAVING 16 x 140
TCH RADIO UNIT
S
3BITS
720BITS
723BITS
S : SEQUENCE NUMBER PROVIDED TO EACH UNITS OBTAINED BY DIVIDING EXTERNAL CODE SYNCHRONIZATION INFORMATION (0 - 7) AND EXTERNAL CODE PROCESSING UNIT (80ms), WITH ASSIGNING SEQUENCE NUMBER 0 TO THE FIRST SELECTION COMBINING UNIT
CRC
TA
13BITS
723BITS
8BITS
2232BITS
DUMMY
8BITS
WRITE
16
140
READ
140
FORWARD TRANSMISSION
WRITE
140
READ
16
REVERSE TRANSMISSION
2240BITS
TCH RADIO UNIT
BIT DEINTERLEAVING 140 X 16
SOFT DECISION VITERBI DECODING R = 1/3K = 9
DISCARD TAIL BITS AND CARRY OUT CRC CHECKING
SELECTION COMBINING
COMBINE SELECTION COMBINING UNITS

FIG.77B

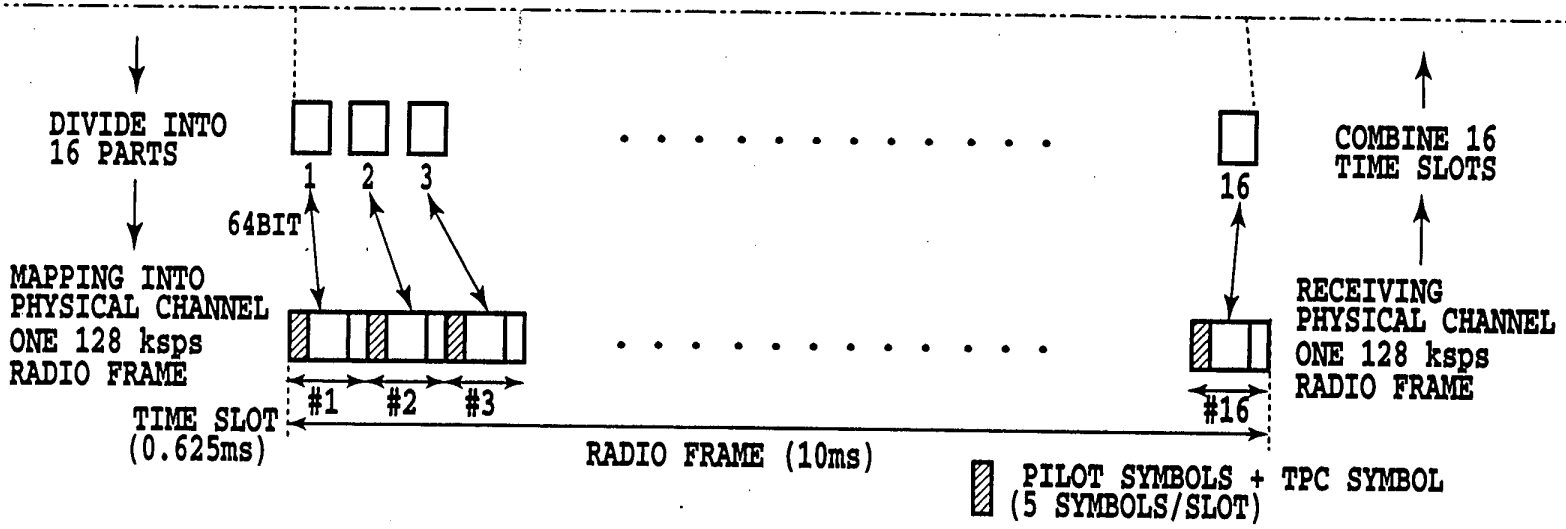

DIVIDE INTO
16 PARTS
MAPPING INTO
PHYSICAL CHANNEL
ONE 128 ksps
RADIO FRAME
64BIT
1
2
3
16
#1
#2
#3
#16
TIME SLOT
(0.625ms)
RADIO FRAME (10ms)
COMBINE 16
TIME SLOTS
RECEIVING
PHYSICAL CHANNEL
ONE 128 ksps
RADIO FRAME
PILOT SYMBOLS + TPC SYMBOL
(5 SYMBOLS/SLOT)

FIG.77C

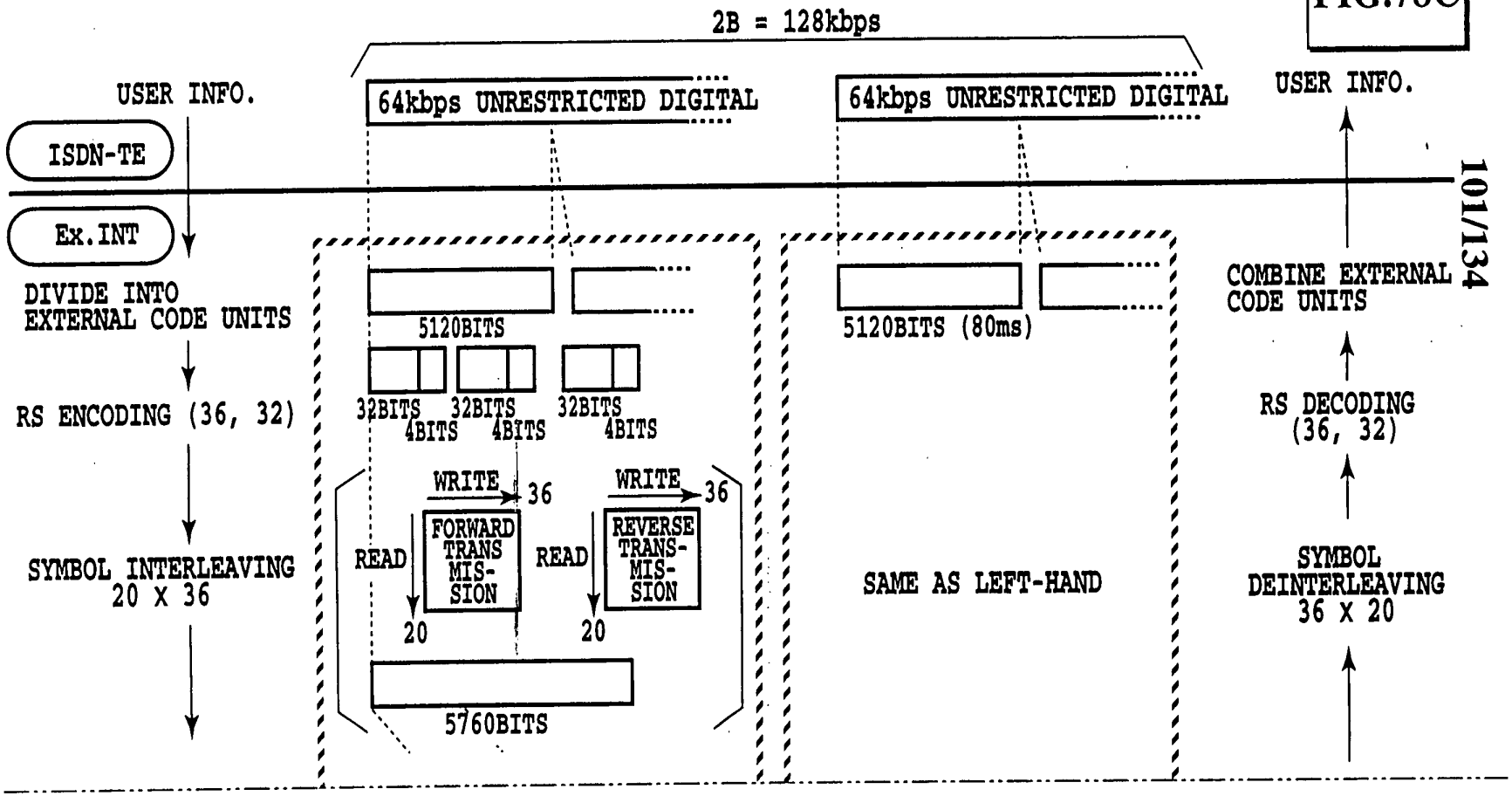
FIG.78

FIG.78A

FIG.78B

FIG.78C

FIG.78A



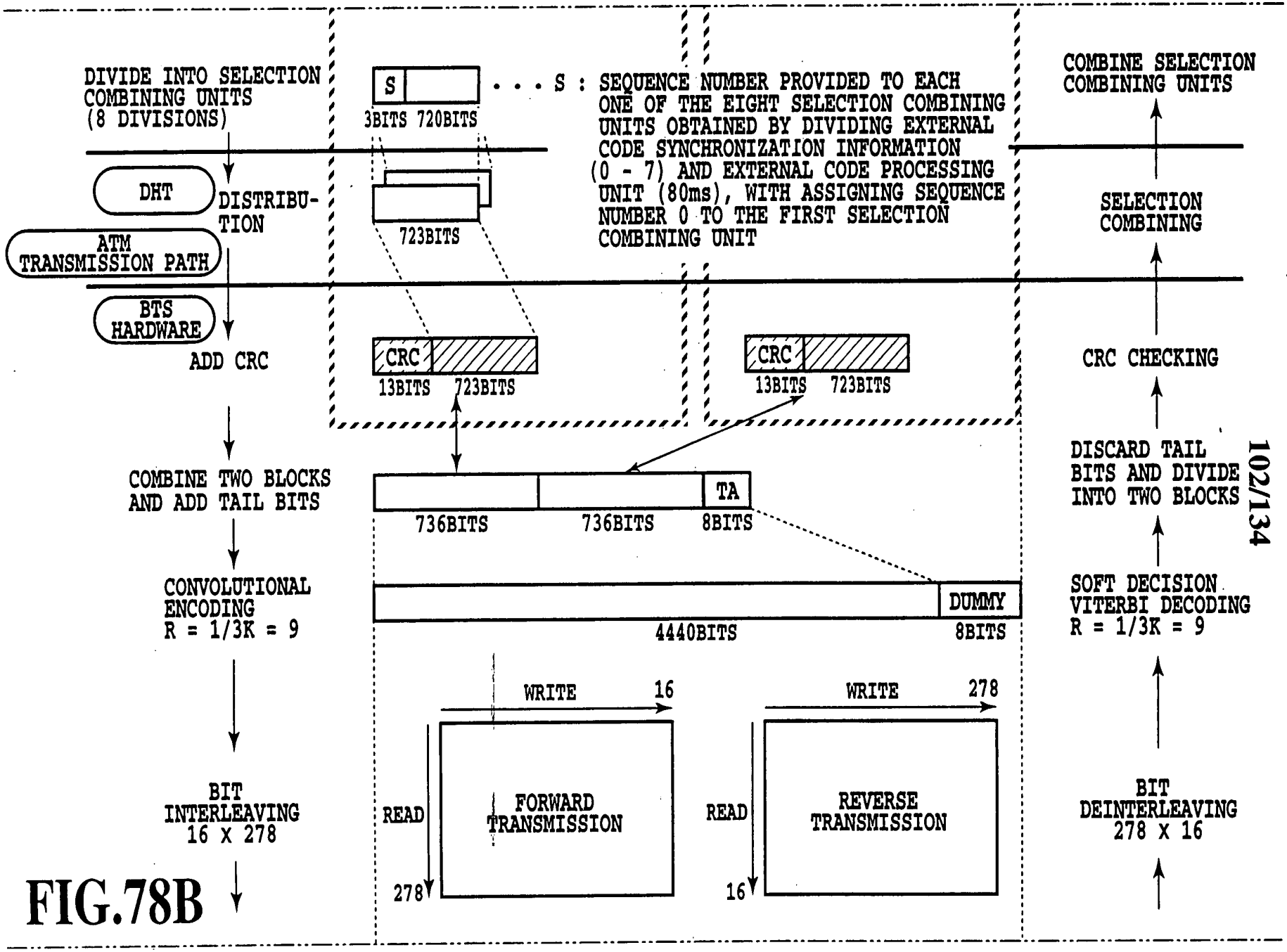

DIVIDE INTO SELECTION COMBINING UNITS (8 DIVISIONS)
S
3BITS 720BITS
. . . S : SEQUENCE NUMBER PROVIDED TO EACH ONE OF THE EIGHT SELECTION COMBINING UNITS OBTAINED BY DIVIDING EXTERNAL CODE SYNCHRONIZATION INFORMATION (0 - 7) AND EXTERNAL CODE PROCESSING UNIT (80ms), WITH ASSIGNING SEQUENCE NUMBER 0 TO THE FIRST SELECTION COMBINING UNIT
COMBINE SELECTION COMBINING UNITS
DHT
DISTRIBU-TION
723BITS
SELECTION COMBINING
ATM TRANSMISSION PATH
BTS HARDWARE
ADD CRC
CRC
13BITS 723BITS
CRC
13BITS 723BITS
CRC CHECKING
COMBINE TWO BLOCKS AND ADD TAIL BITS
TA
736BITS 736BITS 8BITS
DISCARD TAIL BITS AND DIVIDE INTO TWO BLOCKS
CONVOLUTIONAL ENCODING R = 1/3K = 9
DUMMY
4440BITS 8BITS
SOFT DECISION VITERBI DECODING R = 1/3K = 9
WRITE 16
WRITE 278
READ
FORWARD TRANSMISSION
278
READ
REVERSE TRANSMISSION
16
BIT INTERLEAVING 16 x 278
BIT DEINTERLEAVING 278 x 16

FIG.78B

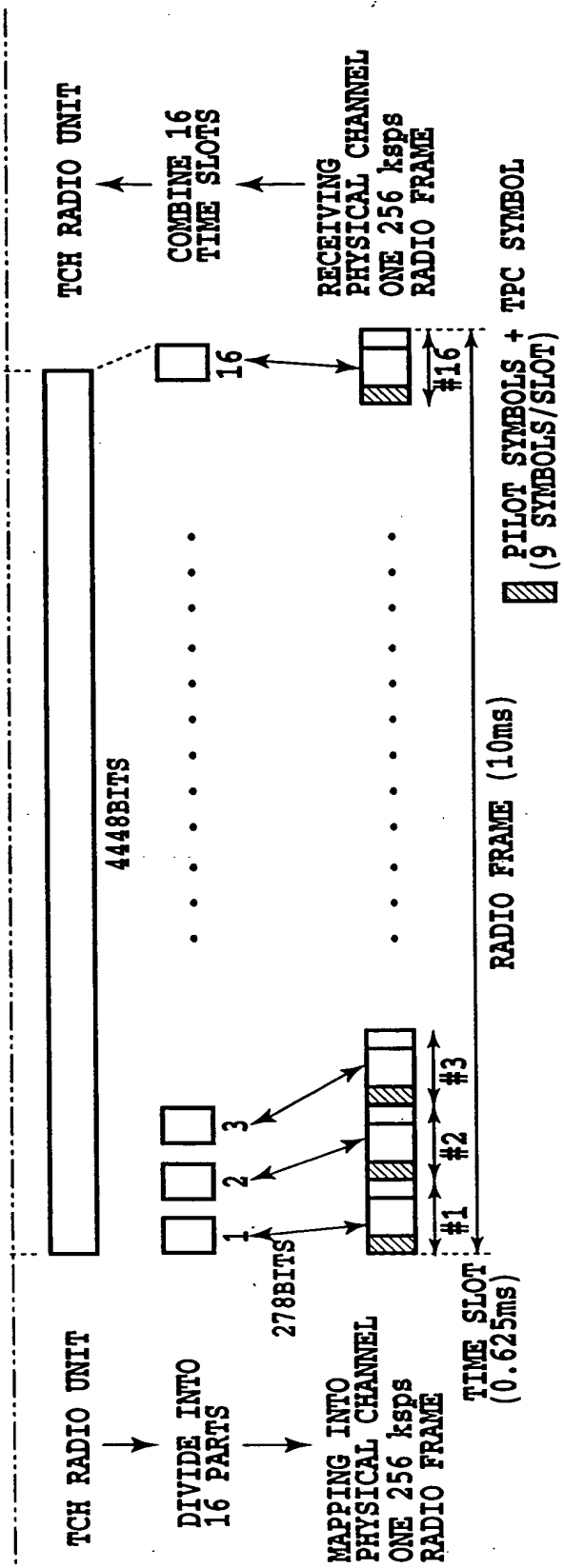

TCH RADIO UNIT
DIVIDE INTO 16 PARTS
MAPPING INTO PHYSICAL CHANNEL ONE 256 ksps RADIO FRAME
278BITS
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS + TPC SYMBOL (9 SYMBOLS/SLOT)
4448BITS
TCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 256 ksps RADIO FRAME
1
2
3
16
#1
#2
#3
#16

FIG.78C

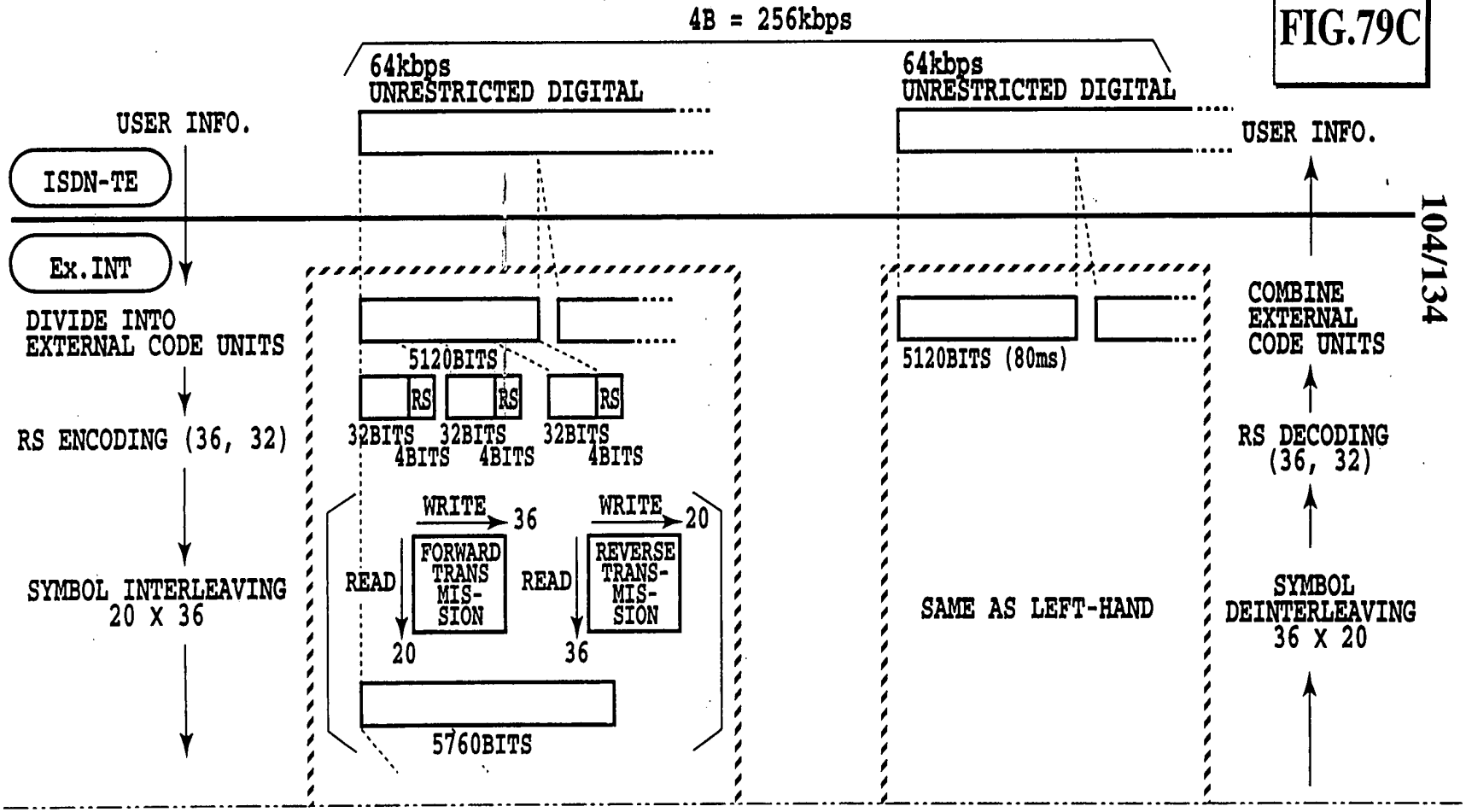
FIG.79

FIG.79A

FIG.79B

FIG.79C

FIG.79A



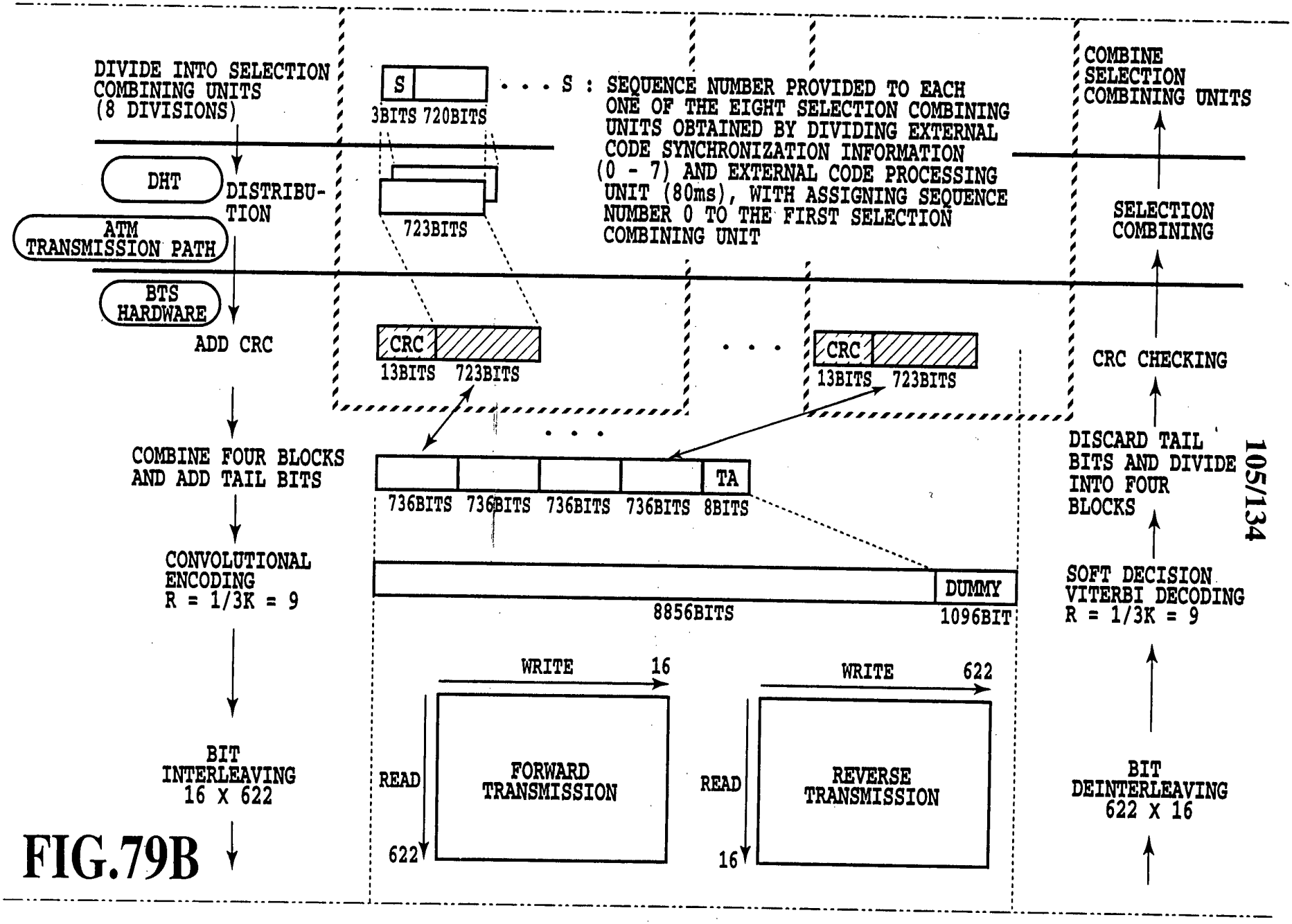

DIVIDE INTO SELECTION COMBINING UNITS (8 DIVISIONS)
S
3BITS 720BITS
. . . S : SEQUENCE NUMBER PROVIDED TO EACH ONE OF THE EIGHT SELECTION COMBINING UNITS OBTAINED BY DIVIDING EXTERNAL CODE SYNCHRONIZATION INFORMATION (0 - 7) AND EXTERNAL CODE PROCESSING UNIT (80ms), WITH ASSIGNING SEQUENCE NUMBER 0 TO THE FIRST SELECTION COMBINING UNIT
COMBINE SELECTION COMBINING UNITS
DHT
DISTRIBU-TION
723BITS
SELECTION COMBINING
ATM TRANSMISSION PATH
BTS HARDWARE
ADD CRC
CRC
13BITS 723BITS
CRC
13BITS 723BITS
CRC CHECKING
COMBINE FOUR BLOCKS AND ADD TAIL BITS
TA
736BITS 736BITS 736BITS 736BITS 8BITS
DISCARD TAIL BITS AND DIVIDE INTO FOUR BLOCKS
CONVOLUTIONAL ENCODING R = 1/3K = 9
DUMMY
8856BITS
1096BIT
SOFT DECISION VITERBI DECODING R = 1/3K = 9
WRITE 16
WRITE 622
READ
FORWARD TRANSMISSION
622
READ
REVERSE TRANSMISSION
16
BIT INTERLEAVING 16 X 622
BIT DEINTERLEAVING 622 X 16

FIG.79B

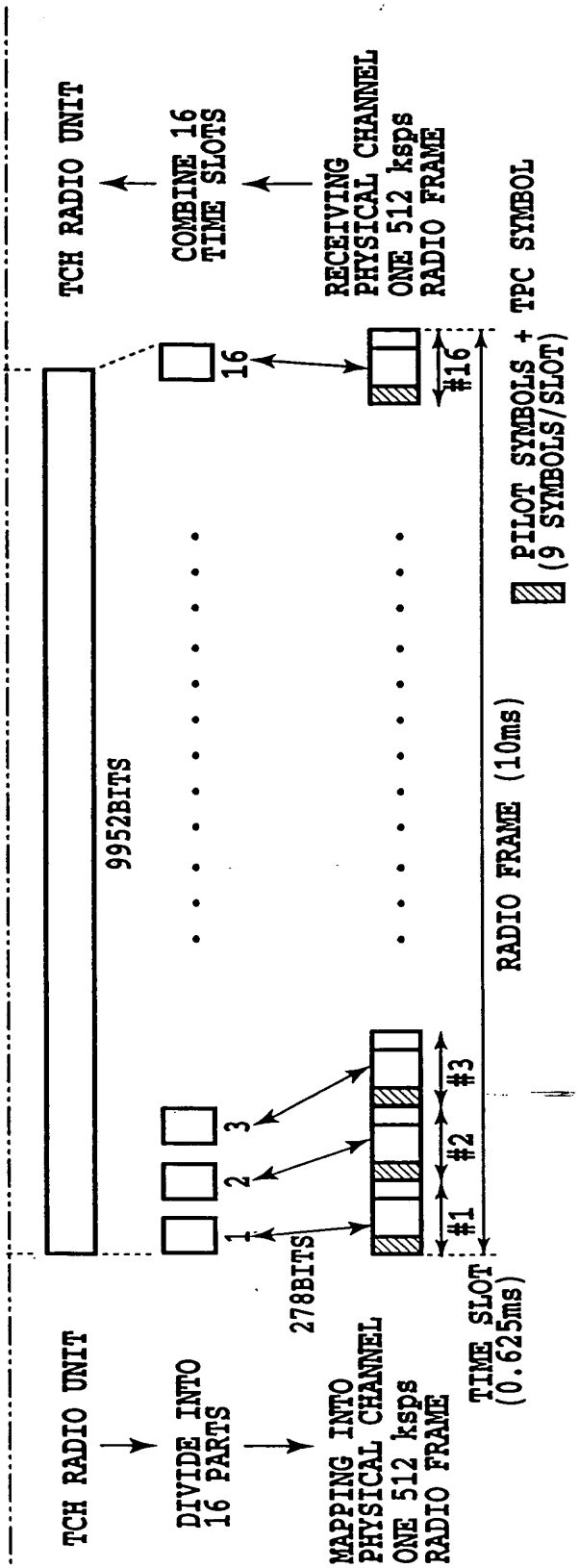

TCH RADIO UNIT
DIVIDE INTO 16 PARTS
MAPPING INTO PHYSICAL CHANNEL ONE 512 ksps RADIO FRAME
278BITS
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
9952BITS
#1
#2
#3
#16
PILOT SYMBOLS + TPC SYMBOL (9 SYMBOLS/SLOT)
RECEIVING PHYSICAL CHANNEL ONE 512 ksps RADIO FRAME
COMBINE 16 TIME SLOTS
TCH RADIO UNIT

FIG.79C

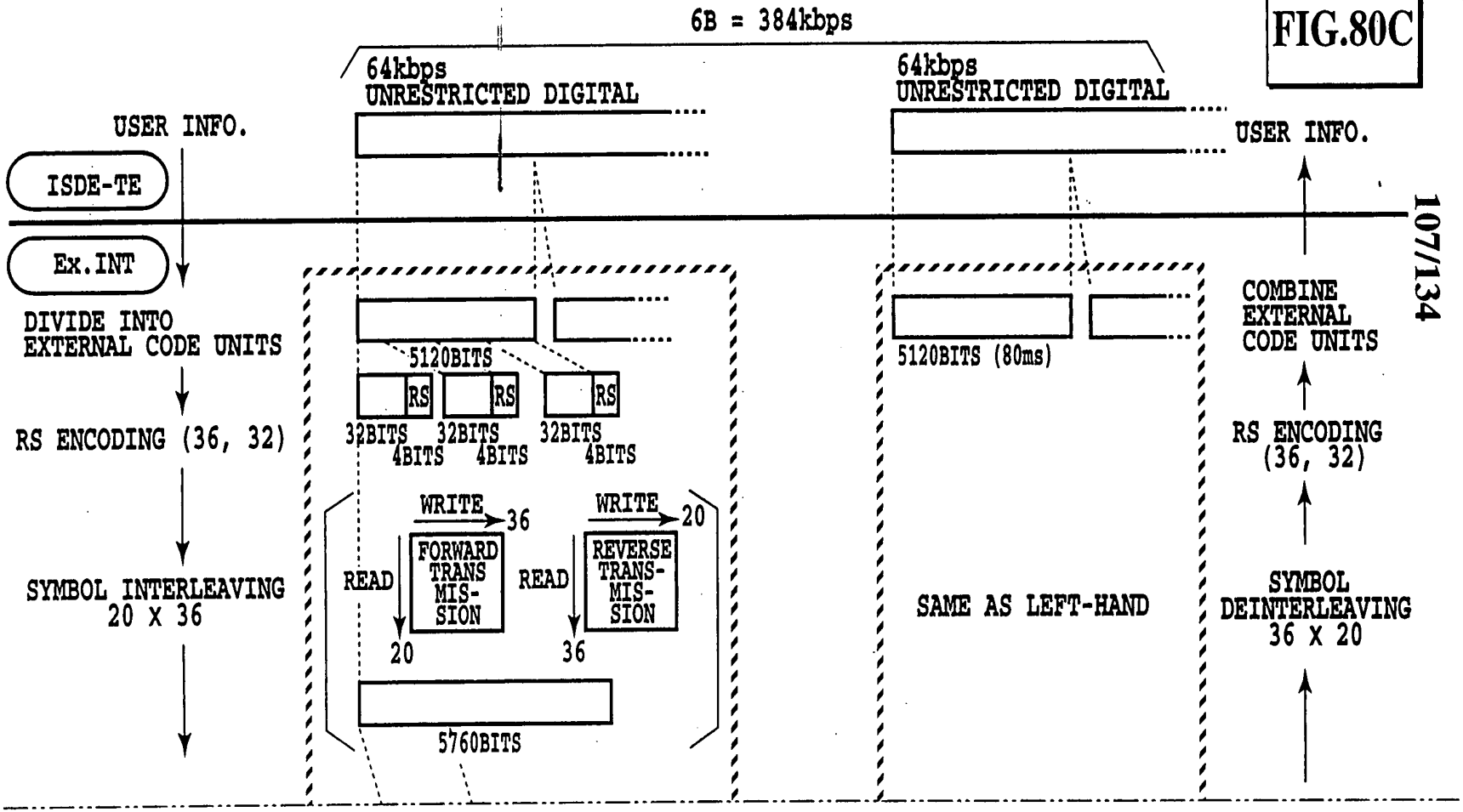
FIG.80

FIG.80A

FIG.80B

FIG.80C

FIG.80A



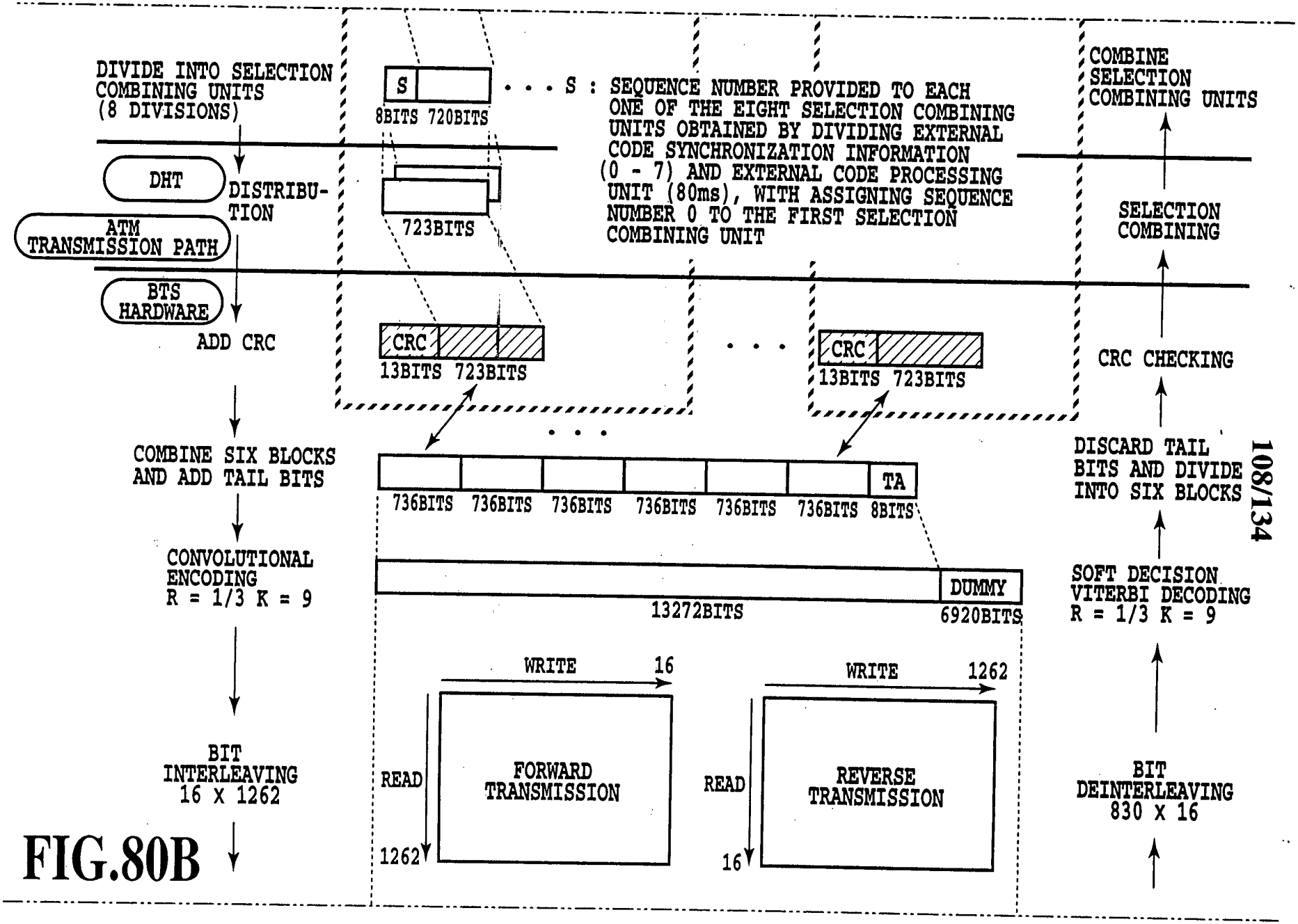

DIVIDE INTO SELECTION COMBINING UNITS (8 DIVISIONS)
S
8BITS 720BITS
. . . S : SEQUENCE NUMBER PROVIDED TO EACH ONE OF THE EIGHT SELECTION COMBINING UNITS OBTAINED BY DIVIDING EXTERNAL CODE SYNCHRONIZATION INFORMATION (0 - 7) AND EXTERNAL CODE PROCESSING UNIT (80ms), WITH ASSIGNING SEQUENCE NUMBER 0 TO THE FIRST SELECTION COMBINING UNIT
COMBINE SELECTION COMBINING UNITS
DHT
DISTRIBU-TION
723BITS
ATM TRANSMISSION PATH
SELECTION COMBINING
BTS HARDWARE
ADD CRC
CRC
13BITS 723BITS
. . .
CRC
13BITS 723BITS
CRC CHECKING
COMBINE SIX BLOCKS AND ADD TAIL BITS
. . .
736BITS 736BITS 736BITS 736BITS 736BITS 736BITS TA 8BITS
DISCARD TAIL BITS AND DIVIDE INTO SIX BLOCKS
CONVOLUTIONAL ENCODING R = 1/3 K = 9
DUMMY
13272BITS
6920BITS
SOFT DECISION VITERBI DECODING R = 1/3 K = 9
WRITE 16
WRITE 1262
READ
FORWARD TRANSMISSION
READ
REVERSE TRANSMISSION
1262
16
BIT INTERLEAVING 16 X 1262
BIT DEINTERLEAVING 830 X 16

FIG.80B

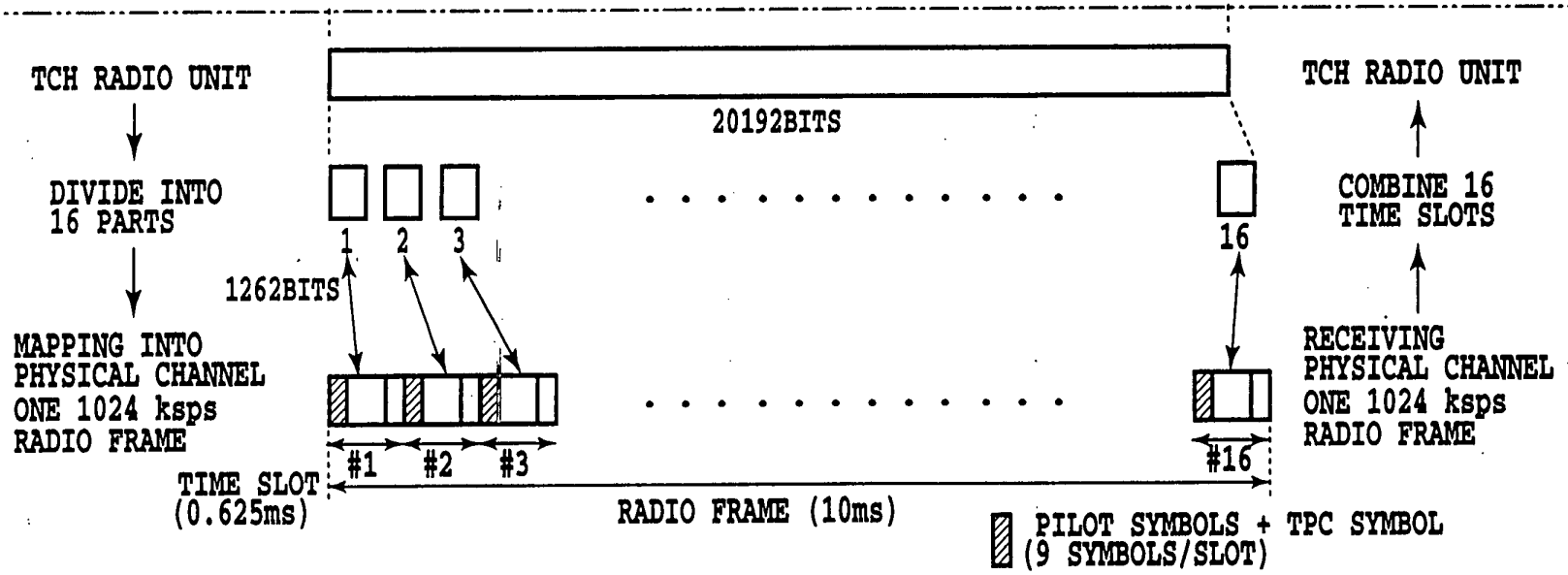

TCH RADIO UNIT
DIVIDE INTO
16 PARTS
MAPPING INTO
PHYSICAL CHANNEL
ONE 1024 ksps
RADIO FRAME
20192BITS
1262BITS
1
2
3
16
#1
#2
#3
#16
TIME SLOT
(0.625ms)
RADIO FRAME (10ms)
TCH RADIO UNIT
COMBINE 16
TIME SLOTS
RECEIVING
PHYSICAL CHANNEL
ONE 1024 ksps
RADIO FRAME
PILOT SYMBOLS + TPC SYMBOL
(9 SYMBOLS/SLOT)

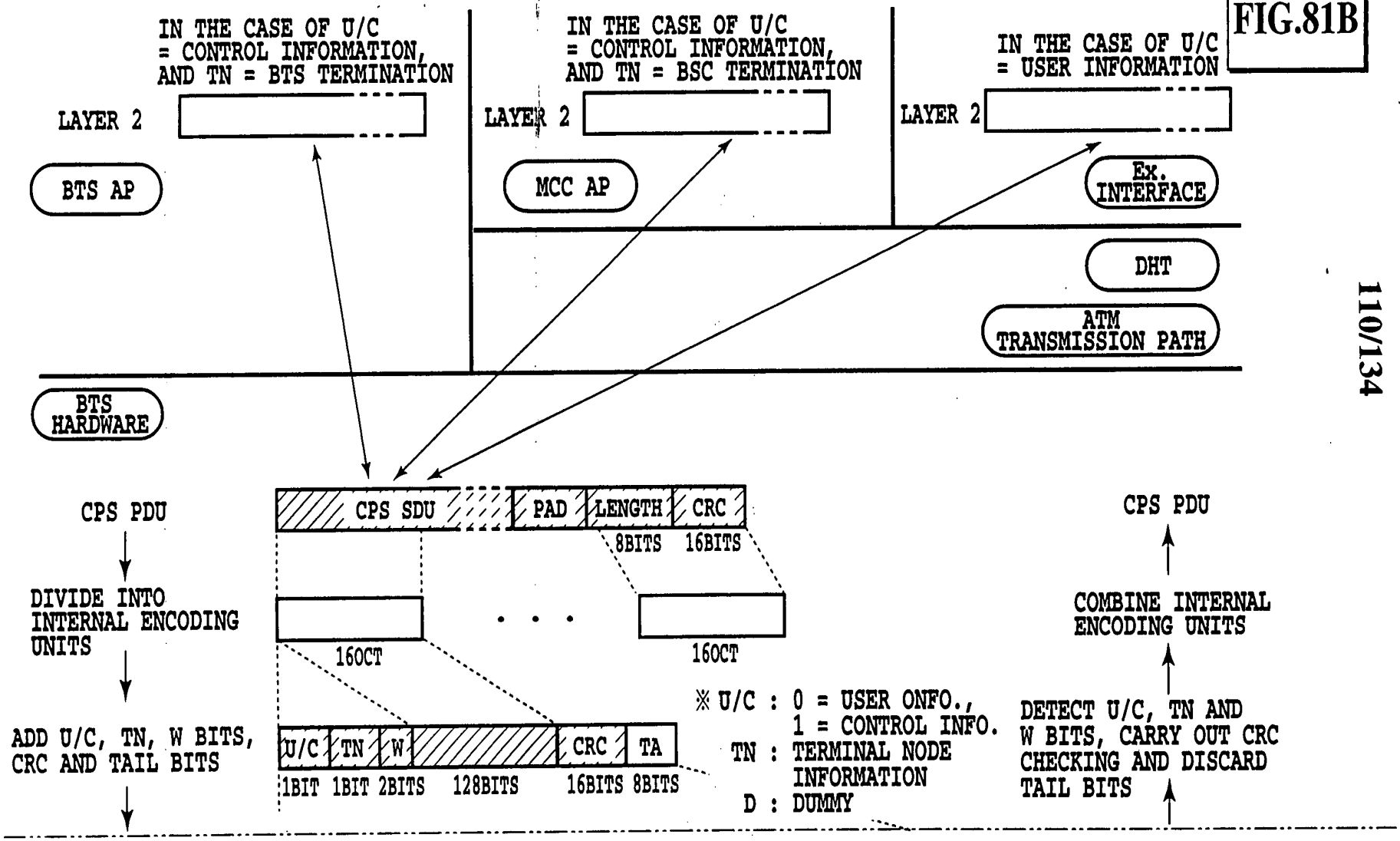
FIG.80C

FIG.81

FIG.81A

FIG.81B

FIG.81A



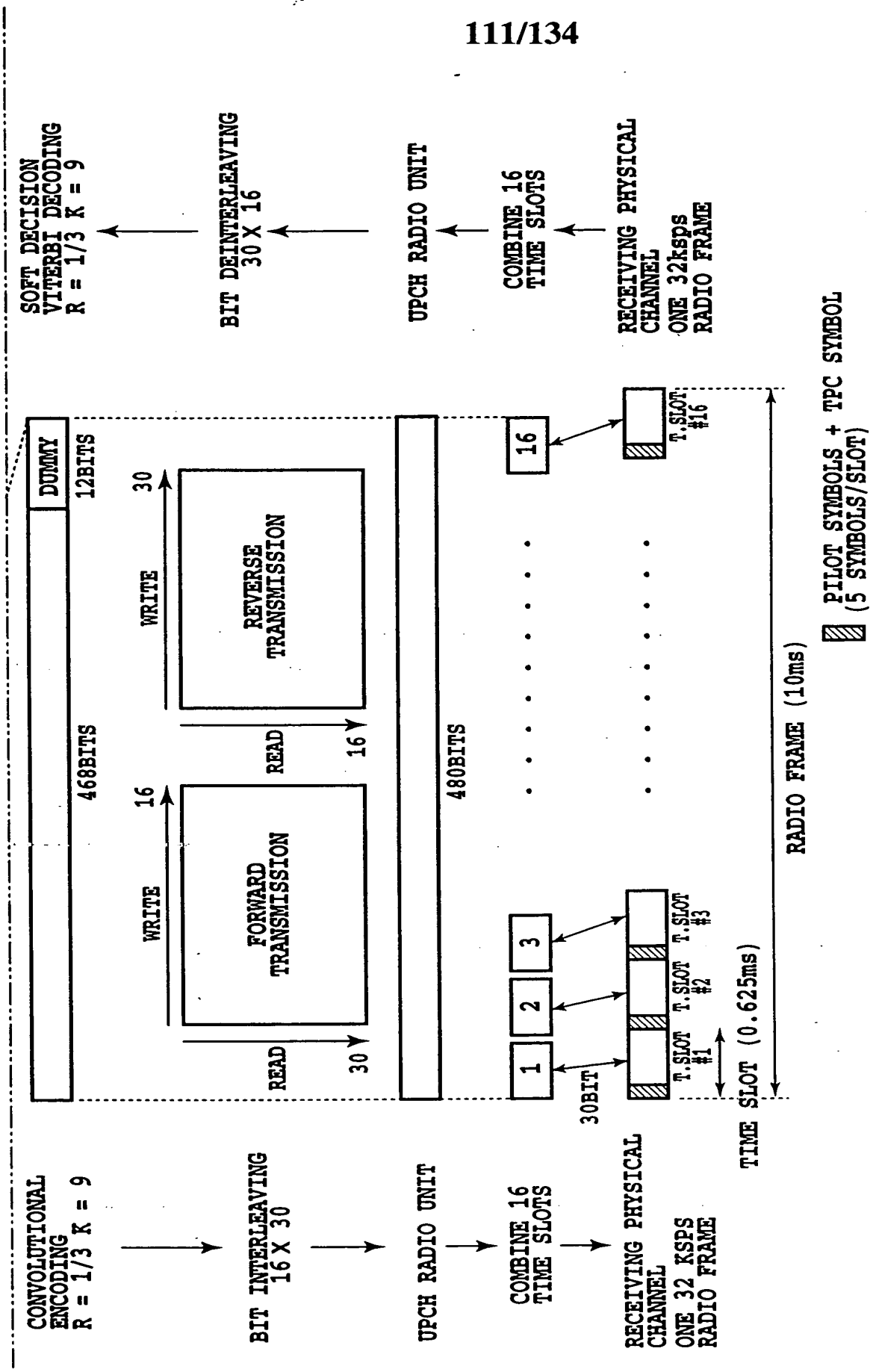

CONVOLUTIONAL ENCODING R = 1/3 K = 9
BIT INTERLEAVING 16 X 30
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 32 KSPS RADIO FRAME
SOFT DECISION VITERBI DECODING R = 1/3 K = 9
BIT DEINTERLEAVING 30 X 16
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 32ksps RADIO FRAME
DUMMY
12BITS
468BITS
WRITE
16
FORWARD TRANSMISSION
READ
30
WRITE
30
REVERSE TRANSMISSION
READ
16
480BITS
1
2
3
30BIT
T.SLOT #1
T.SLOT #2
T.SLOT #3
16
T.SLOT #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)

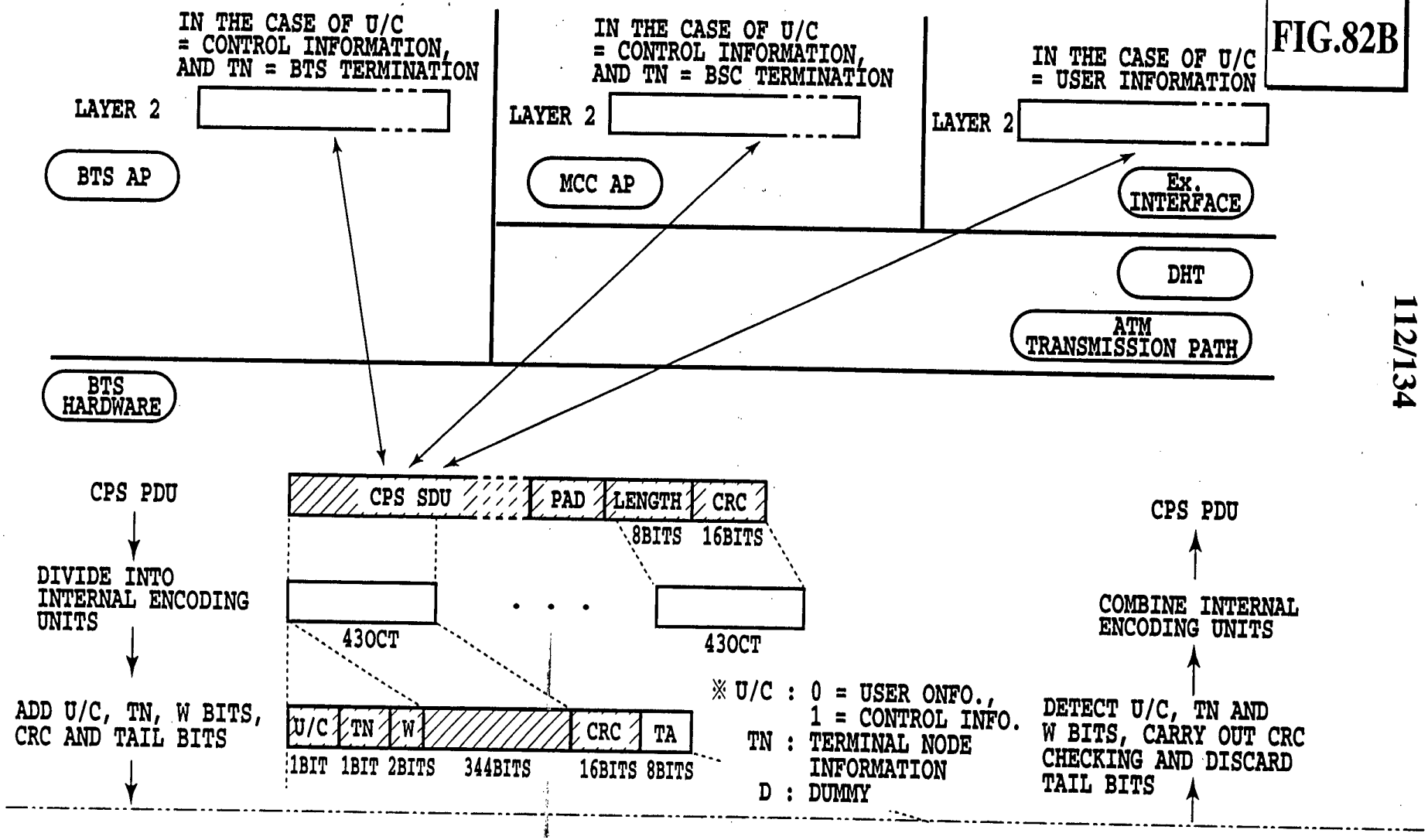
FIG.81B

FIG.82

FIG.82A

FIG.82B

FIG.82A



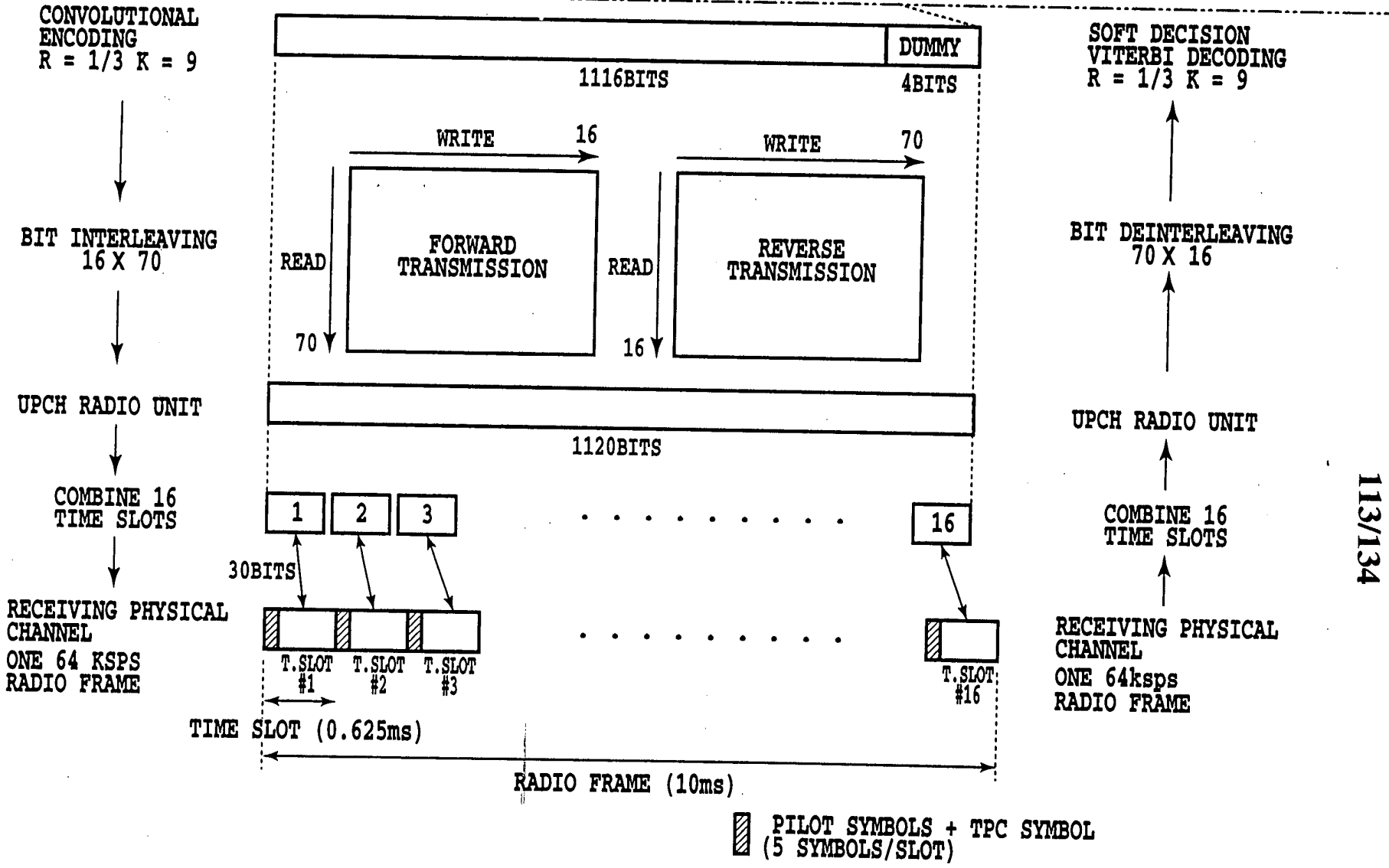

CONVOLUTIONAL ENCODING R = 1/3 K = 9
BIT INTERLEAVING 16 X 70
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL
ONE 64 KSPS RADIO FRAME
1116BITS
DUMMY
4BITS
WRITE
16
WRITE
70
READ
70
FORWARD TRANSMISSION
READ
16
REVERSE TRANSMISSION
1120BITS
1
2
3
16
30BITS
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)
SOFT DECISION VITERBI DECODING R = 1/3 K = 9
BIT DEINTERLEAVING 70 X 16
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL
ONE 64ksps RADIO FRAME

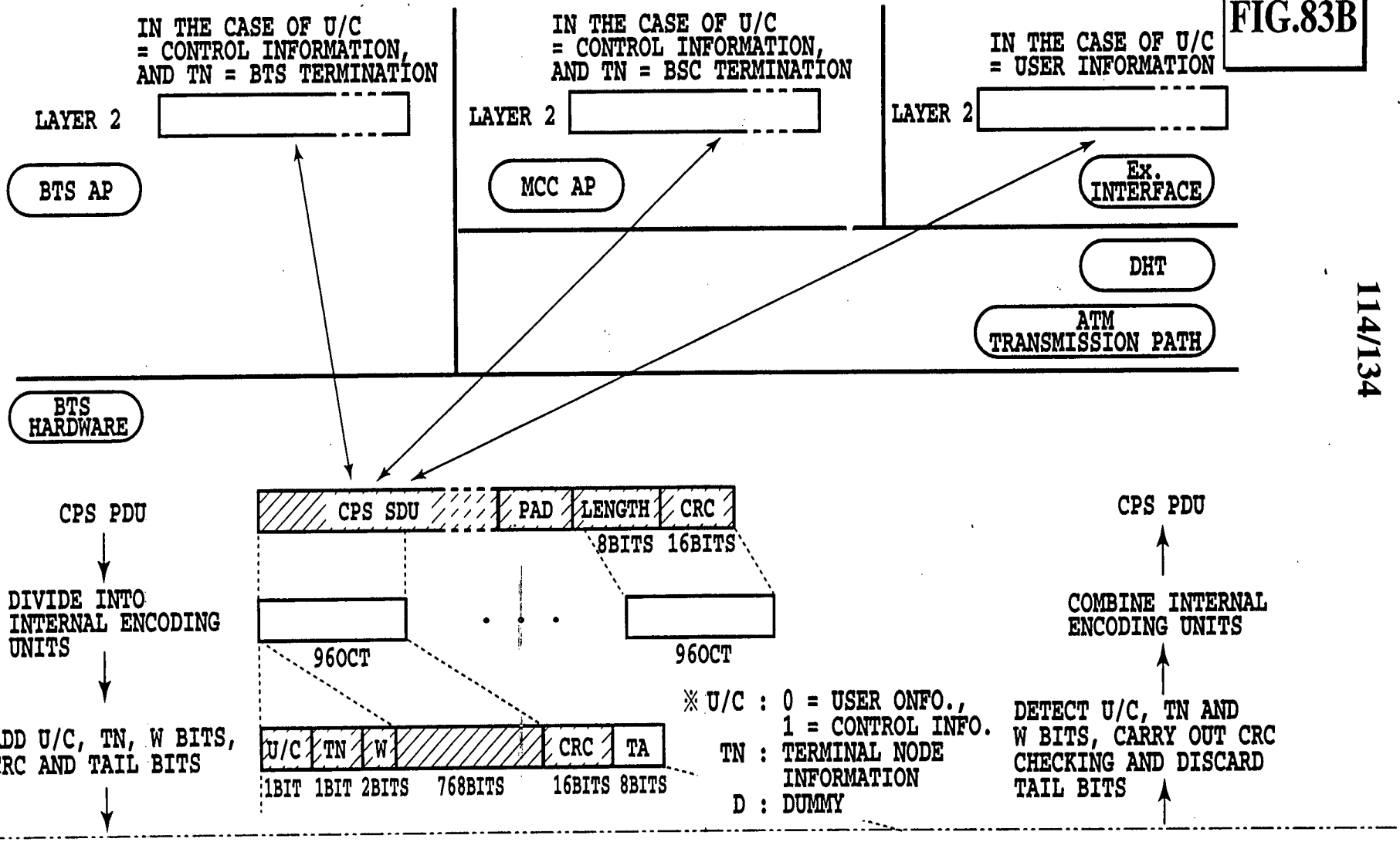
FIG.82B

FIG.83

FIG.83A

FIG.83B

FIG.83A



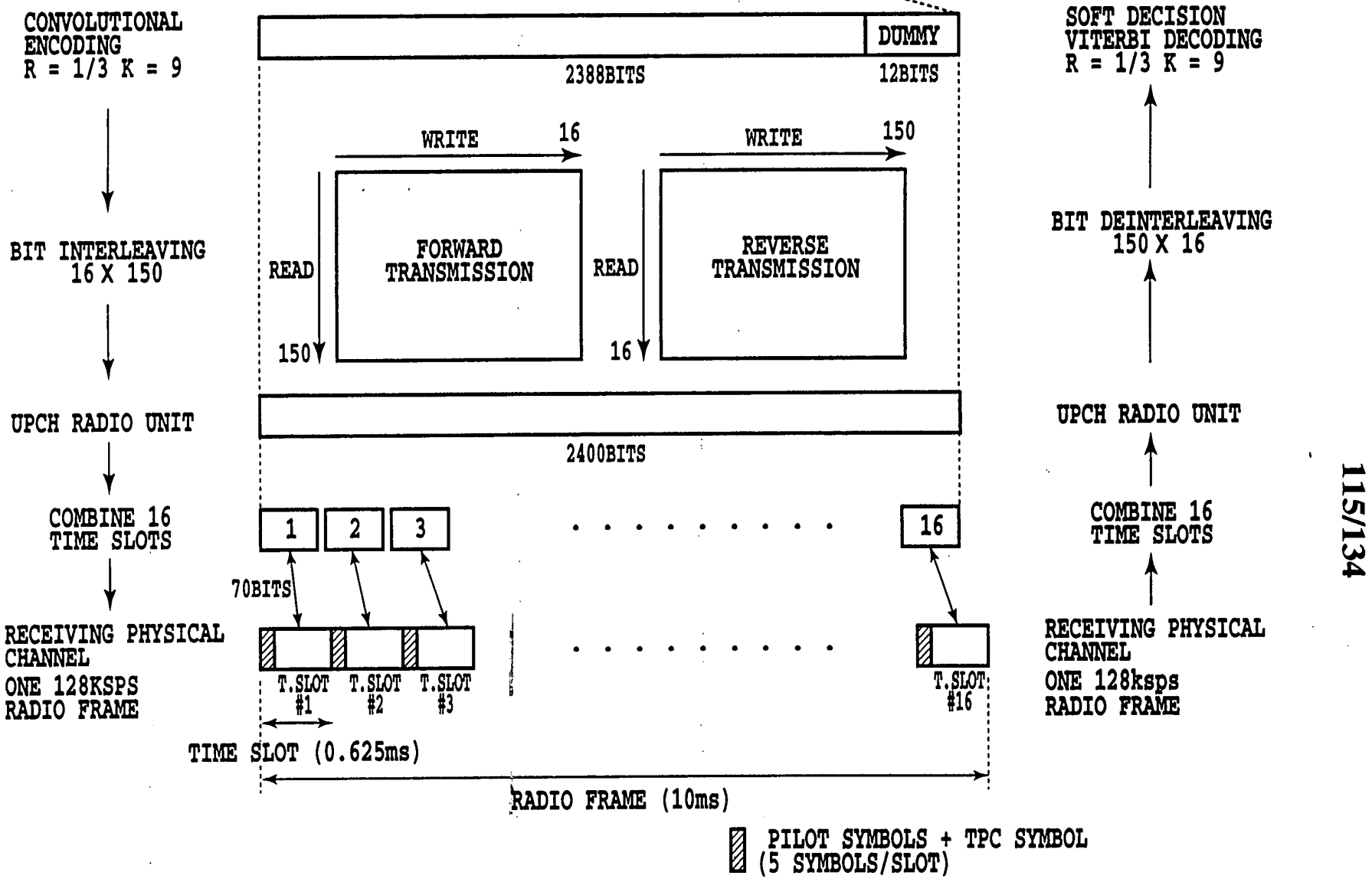

CONVOLUTIONAL ENCODING R = 1/3 K = 9
BIT INTERLEAVING 16 X 150
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 128KSPS RADIO FRAME
DUMMY
2388BITS
12BITS
WRITE
16
WRITE
150
READ
150
FORWARD TRANSMISSION
READ
16
REVERSE TRANSMISSION
2400BITS
1
2
3
16
70BITS
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS + TPC SYMBOL (5 SYMBOLS/SLOT)
SOFT DECISION VITERBI DECODING R = 1/3 K = 9
BIT DEINTERLEAVING 150 X 16
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 128ksps RADIO FRAME

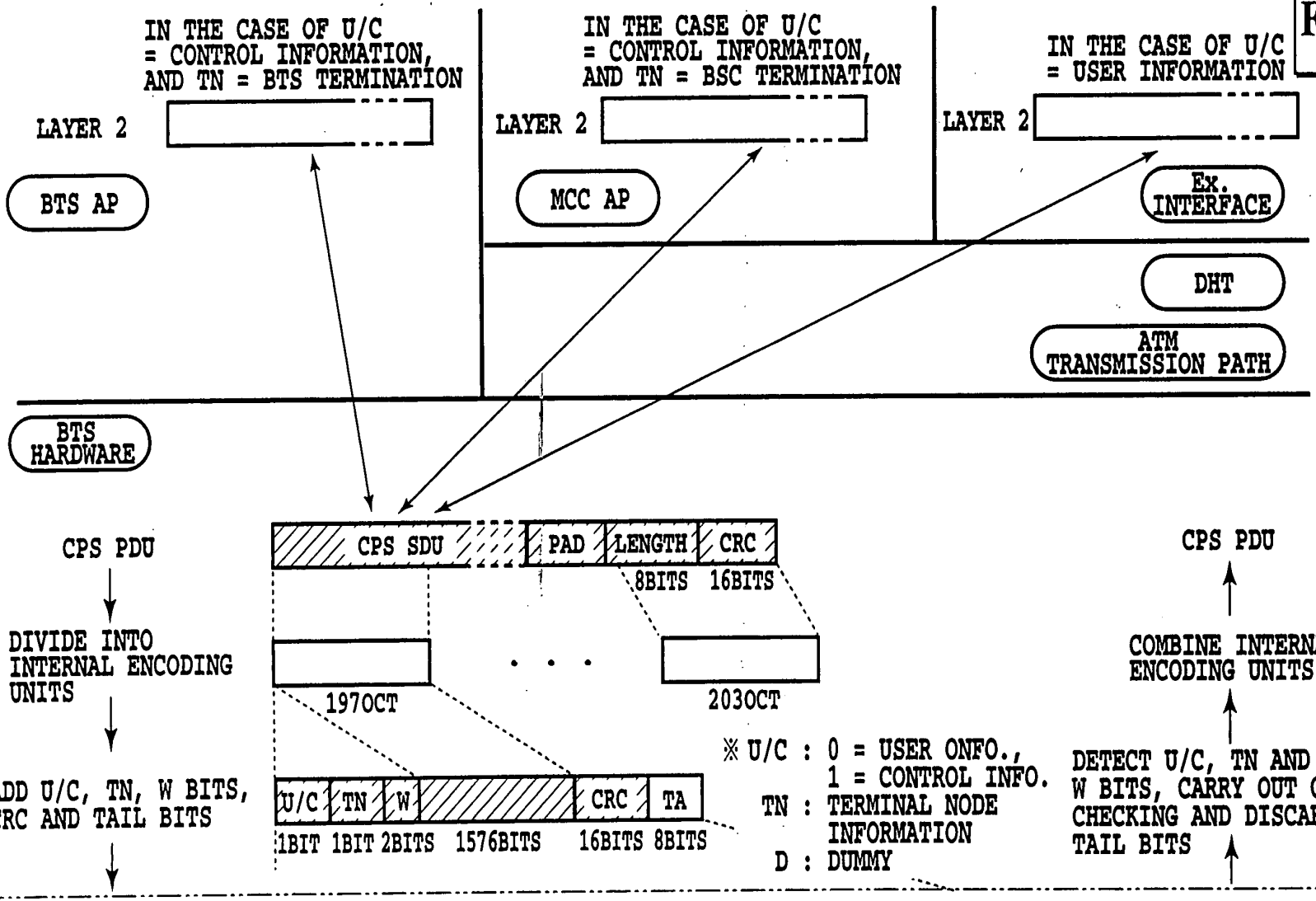
FIG.83B

FIG.84

FIG.84A

FIG.84B

FIG.84A



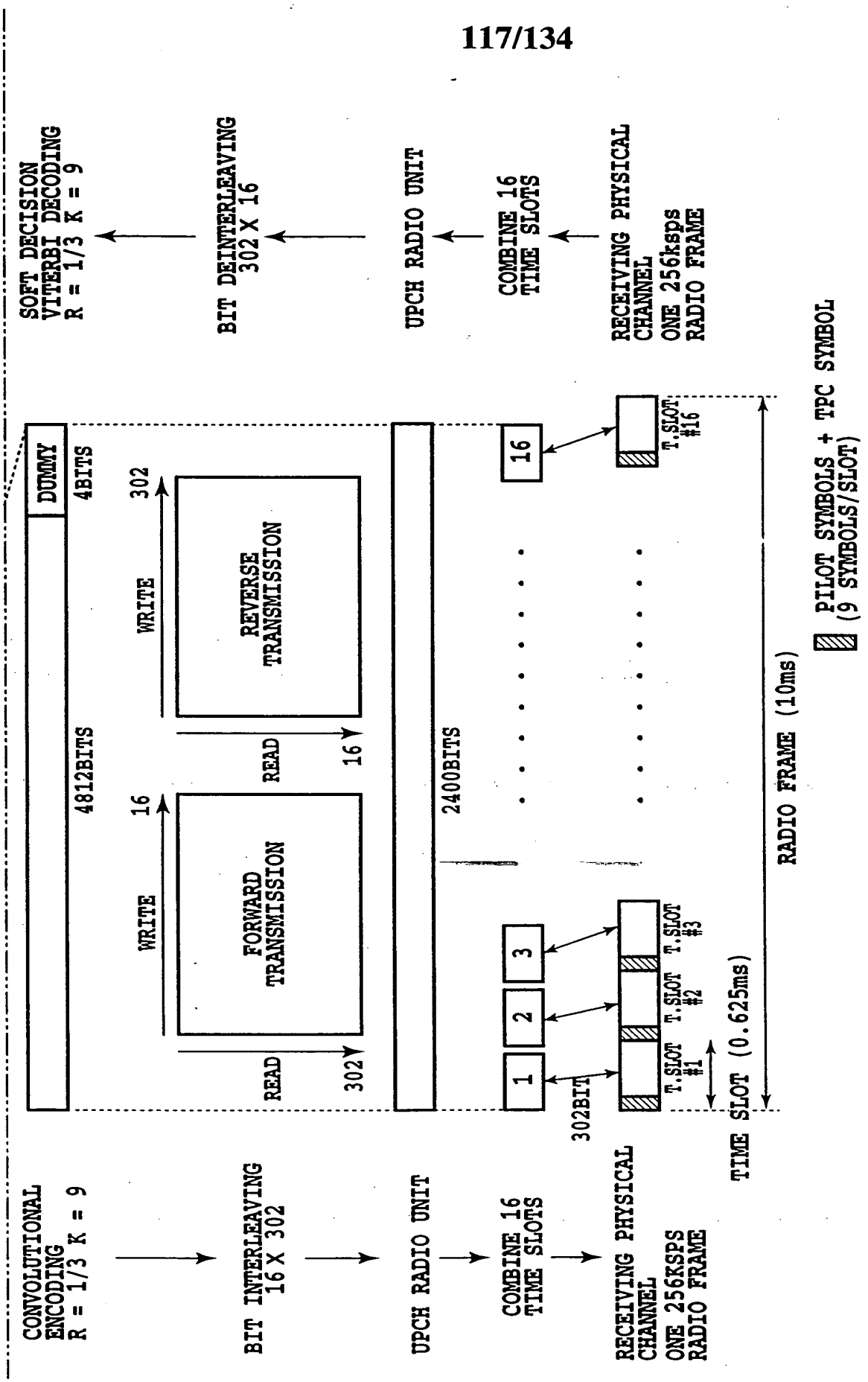

CONVOLUTIONAL ENCODING R = 1/3 K = 9
BIT INTERLEAVING 16 X 302
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 256KSPS RADIO FRAME
SOFT DECISION VITERBI DECODING R = 1/3 K = 9
BIT DEINTERLEAVING 302 X 16
UPCH RADIO UNIT
COMBINE 16 TIME SLOTS
RECEIVING PHYSICAL CHANNEL ONE 256ksps RADIO FRAME
DUMMY
4BITS
4812BITS
WRITE
16
FORWARD TRANSMISSION
READ
302
WRITE
302
REVERSE TRANSMISSION
READ
16
2400BITS
1
2
3
16
302BIT
T.SLOT #1
T.SLOT #2
T.SLOT #3
T.SLOT #16
TIME SLOT (0.625ms)
RADIO FRAME (10ms)
PILOT SYMBOLS + TPC SYMBOL (9 SYMBOLS/SLOT)

FIG.84B

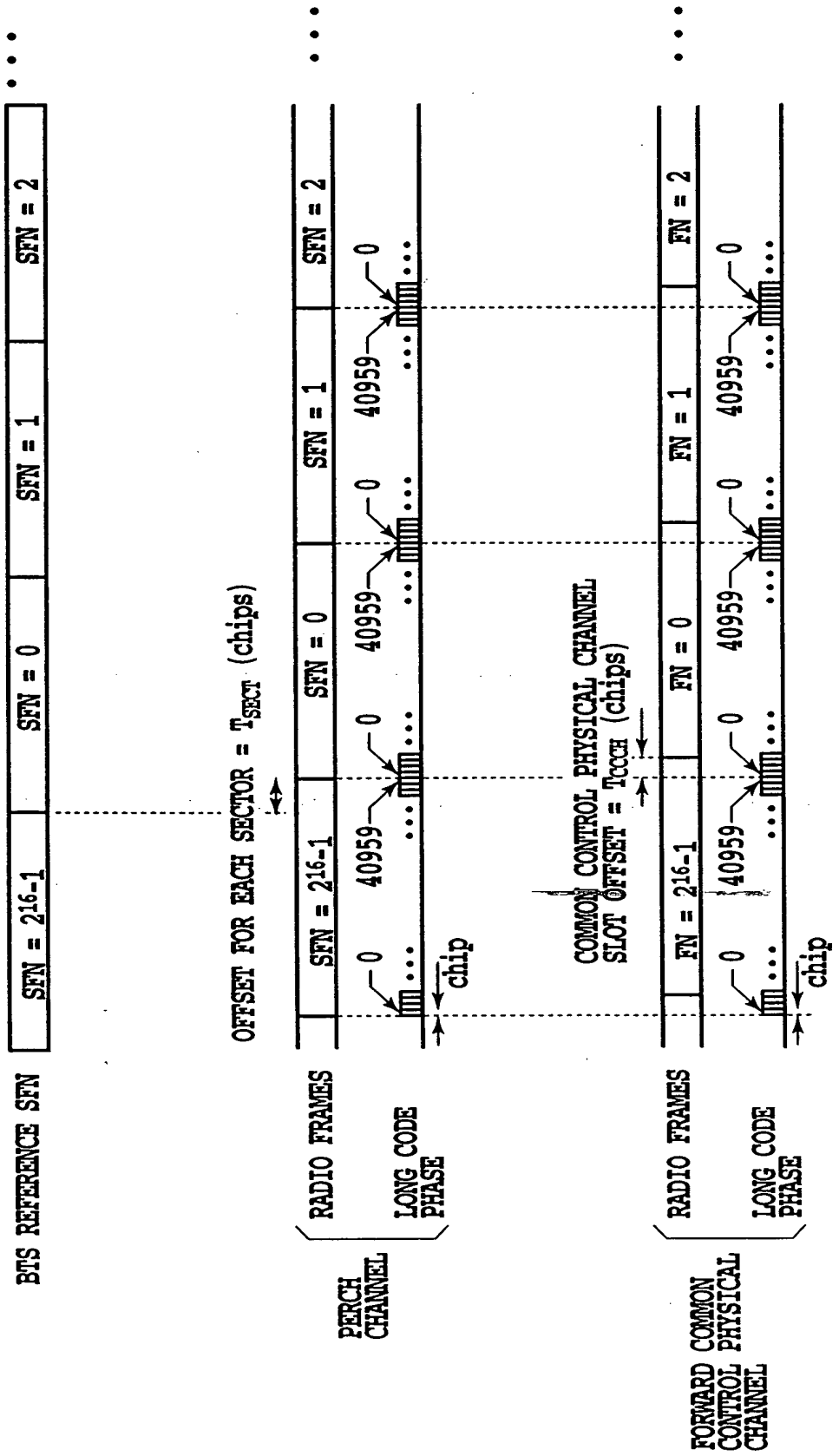

BTS REFERENCE SFN
SFN = 2^16-1
SFN = 0
SFN = 1
SFN = 2
OFFSET FOR EACH SECTOR = T_SECT (chips)
PERCH CHANNEL
RADIO FRAMES
LONG CODE PHASE
chip
0
40959
COMMON CONTROL PHYSICAL CHANNEL SLOT OFFSET = T_CCCH (chips)
FORWARD COMMON CONTROL PHYSICAL CHANNEL
FN = 2^16-1
FN = 0
FN = 1
FN = 2

FIG.85

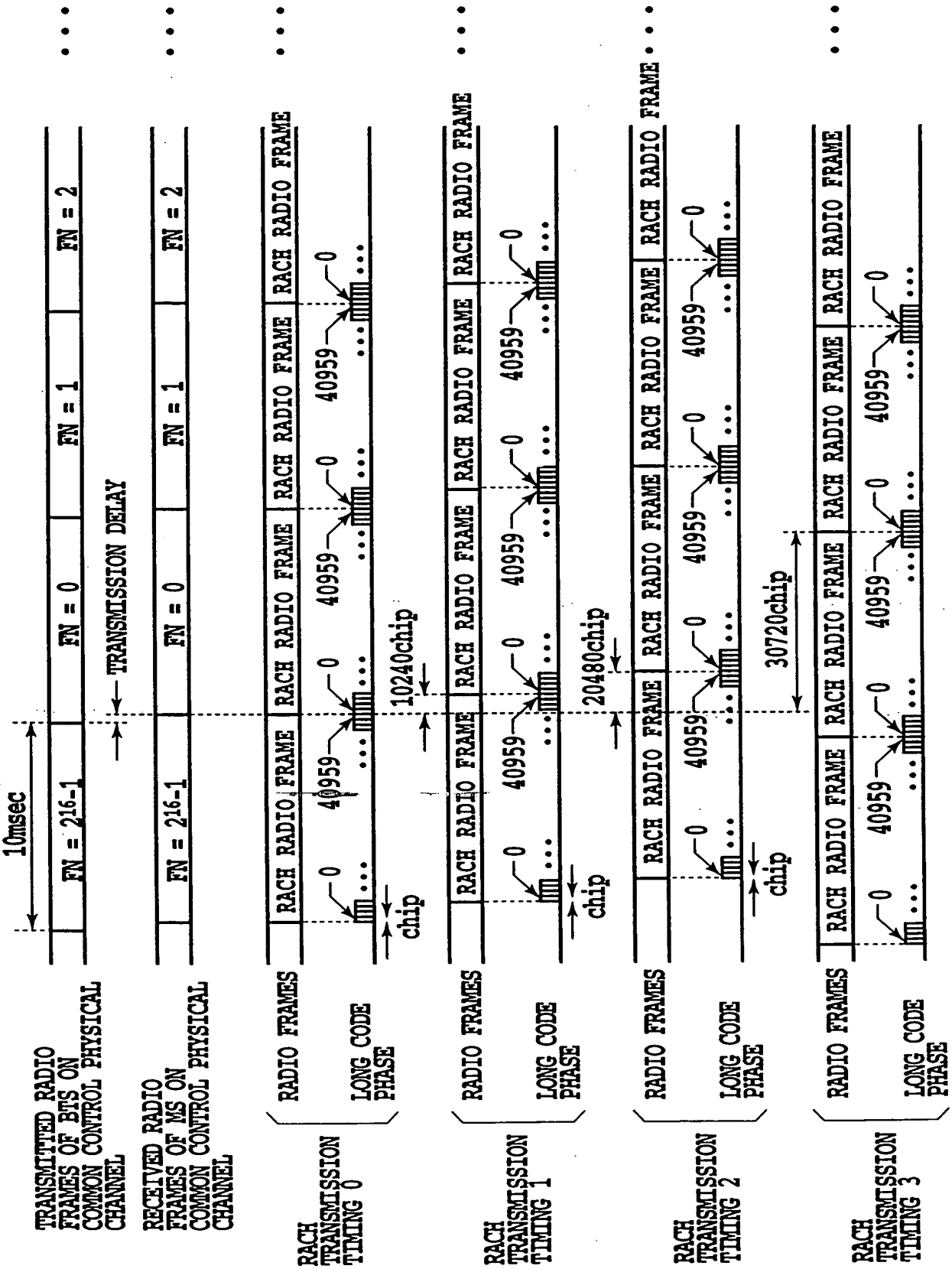

10msec
TRANSMITTED RADIO FRAMES OF BTS ON COMMON CONTROL PHYSICAL CHANNEL
FN = 2^16-1
FN = 0
FN = 1
FN = 2
TRANSMISSION DELAY
RECEIVED RADIO FRAMES OF MS ON COMMON CONTROL PHYSICAL CHANNEL
RACH RADIO FRAME
RADIO FRAMES
LONG CODE PHASE
RACH TRANSMISSION TIMING 0
RACH TRANSMISSION TIMING 1
RACH TRANSMISSION TIMING 2
RACH TRANSMISSION TIMING 3
0
40959
chip
10240chip
20480chip
30720chip

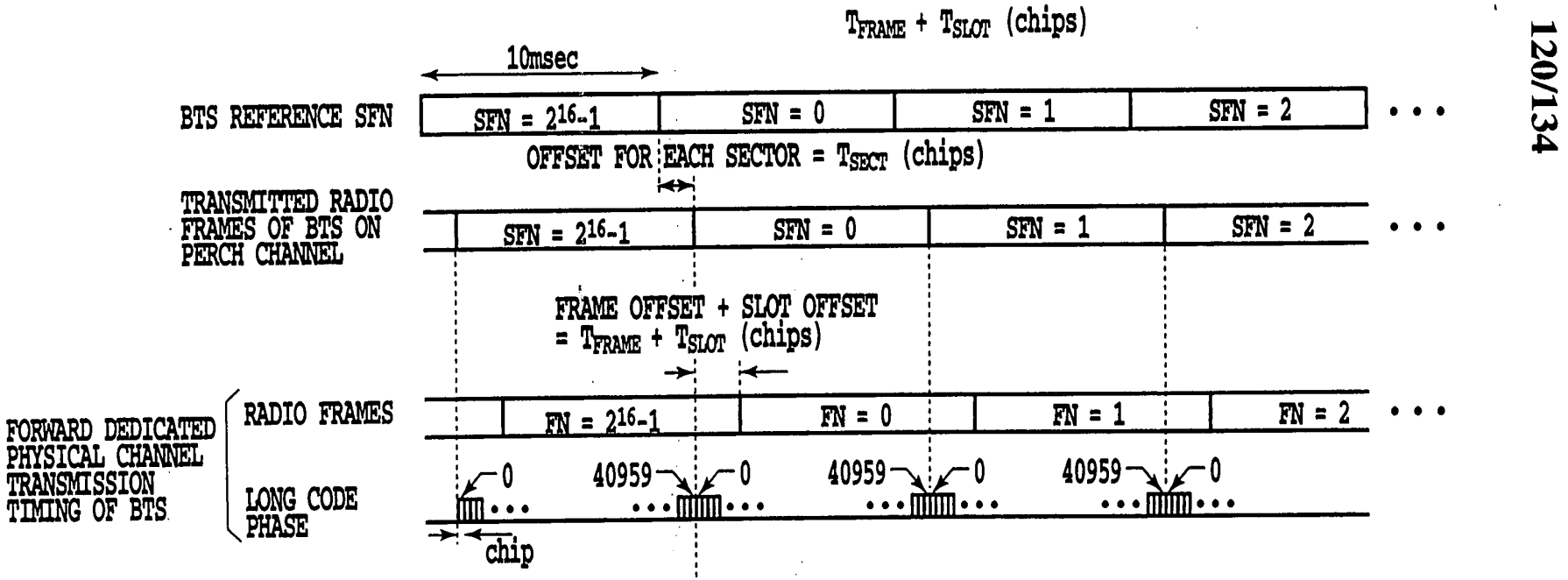
FIG.86

FIG.87

FIG.87A

FIG.87B

FIG.87A



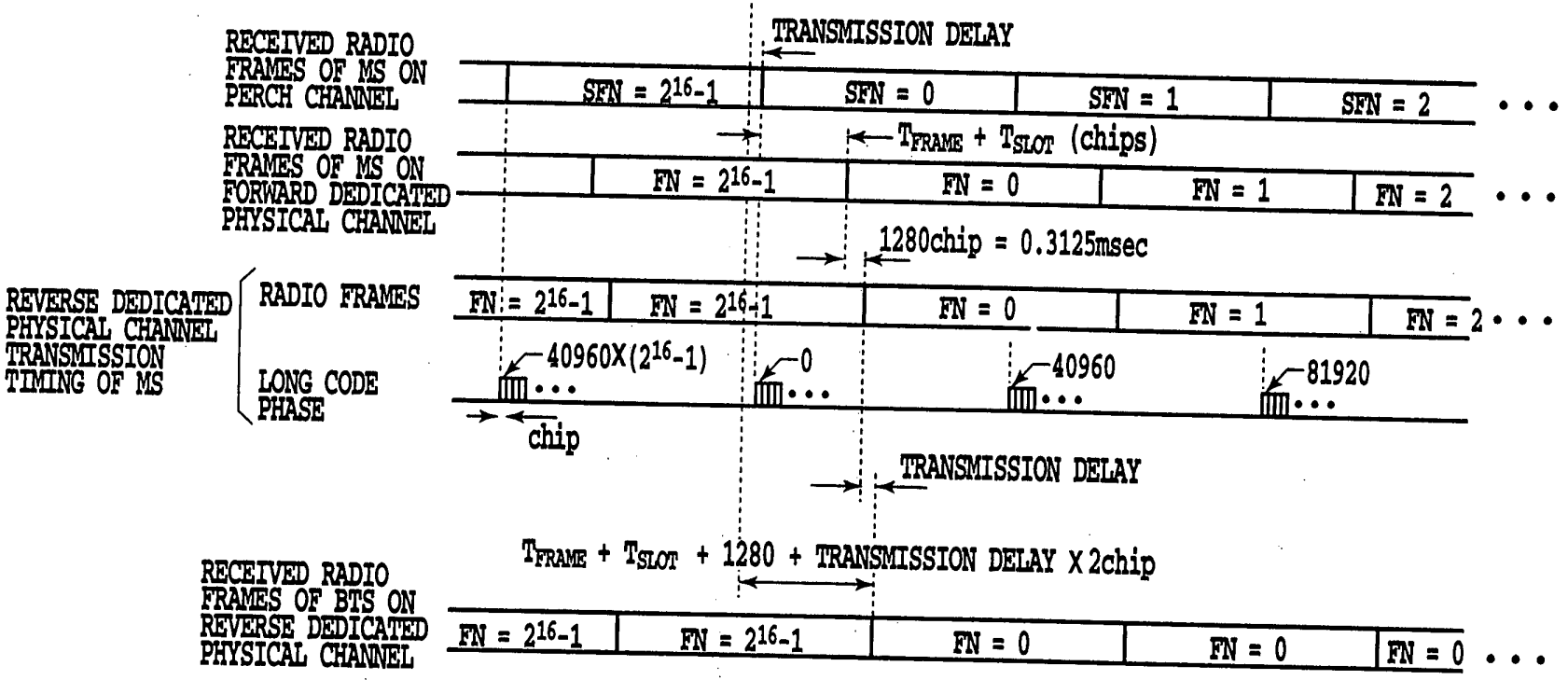

RECEIVED RADIO FRAMES OF MS ON PERCH CHANNEL
TRANSMISSION DELAY
SFN = 2^16-1
SFN = 0
SFN = 1
SFN = 2
RECEIVED RADIO FRAMES OF MS ON FORWARD DEDICATED PHYSICAL CHANNEL
T_FRAME + T_SLOT (chips)
FN = 2^16-1
FN = 0
FN = 1
FN = 2
1280chip = 0.3125msec
REVERSE DEDICATED PHYSICAL CHANNEL TRANSMISSION TIMING OF MS
RADIO FRAMES
FN = 2^16-1
FN = 2^16-1
FN = 0
FN = 1
FN = 2
LONG CODE PHASE
40960X(2^16-1)
0
40960
81920
chip
TRANSMISSION DELAY
T_FRAME + T_SLOT + 1280 + TRANSMISSION DELAY X 2chip
RECEIVED RADIO FRAMES OF BTS ON REVERSE DEDICATED PHYSICAL CHANNEL
FN = 2^16-1
FN = 2^16-1
FN = 0
FN = 0
FN = 0

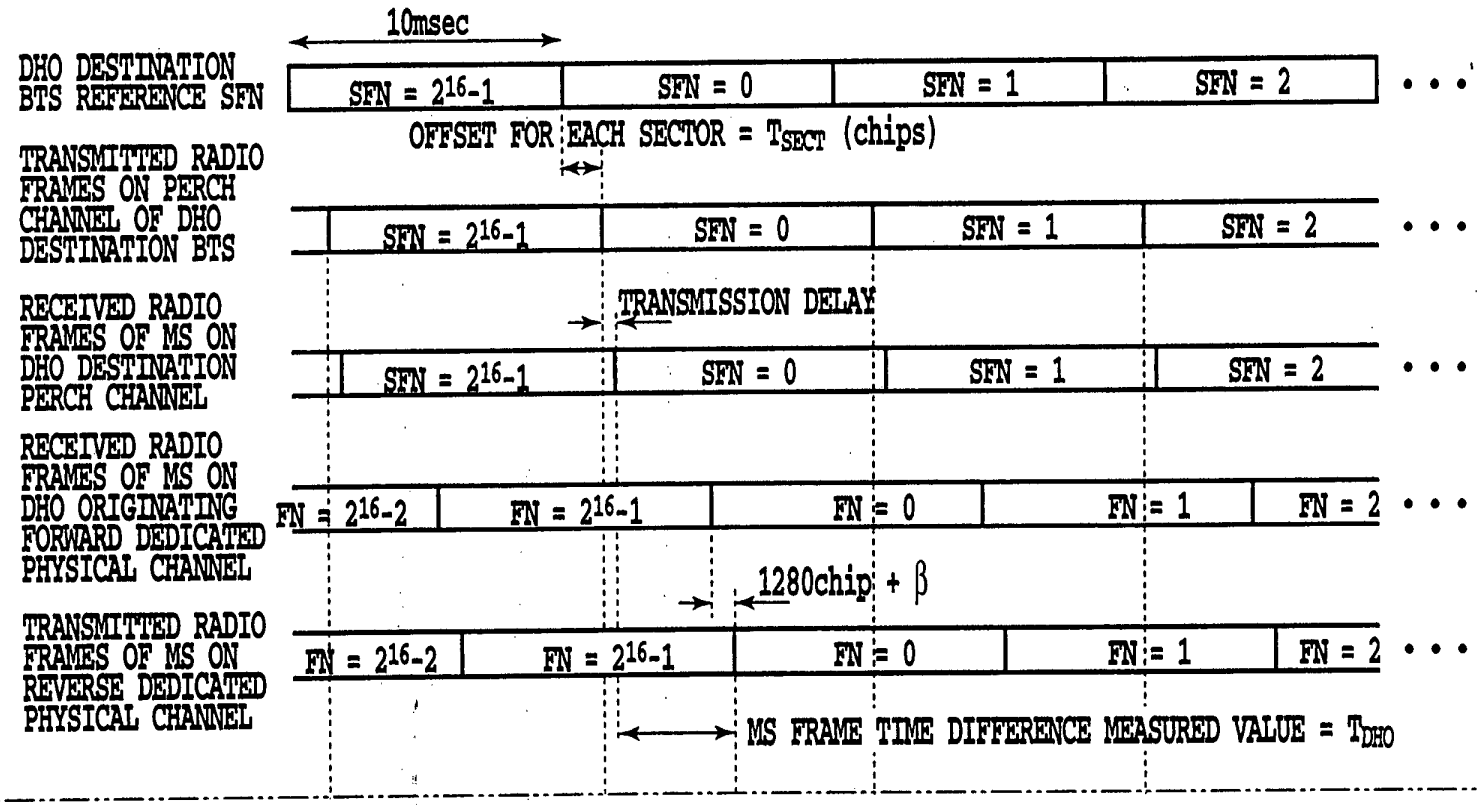
FIG.87B

FIG.88

FIG.88A

FIG.88B

FIG.88A



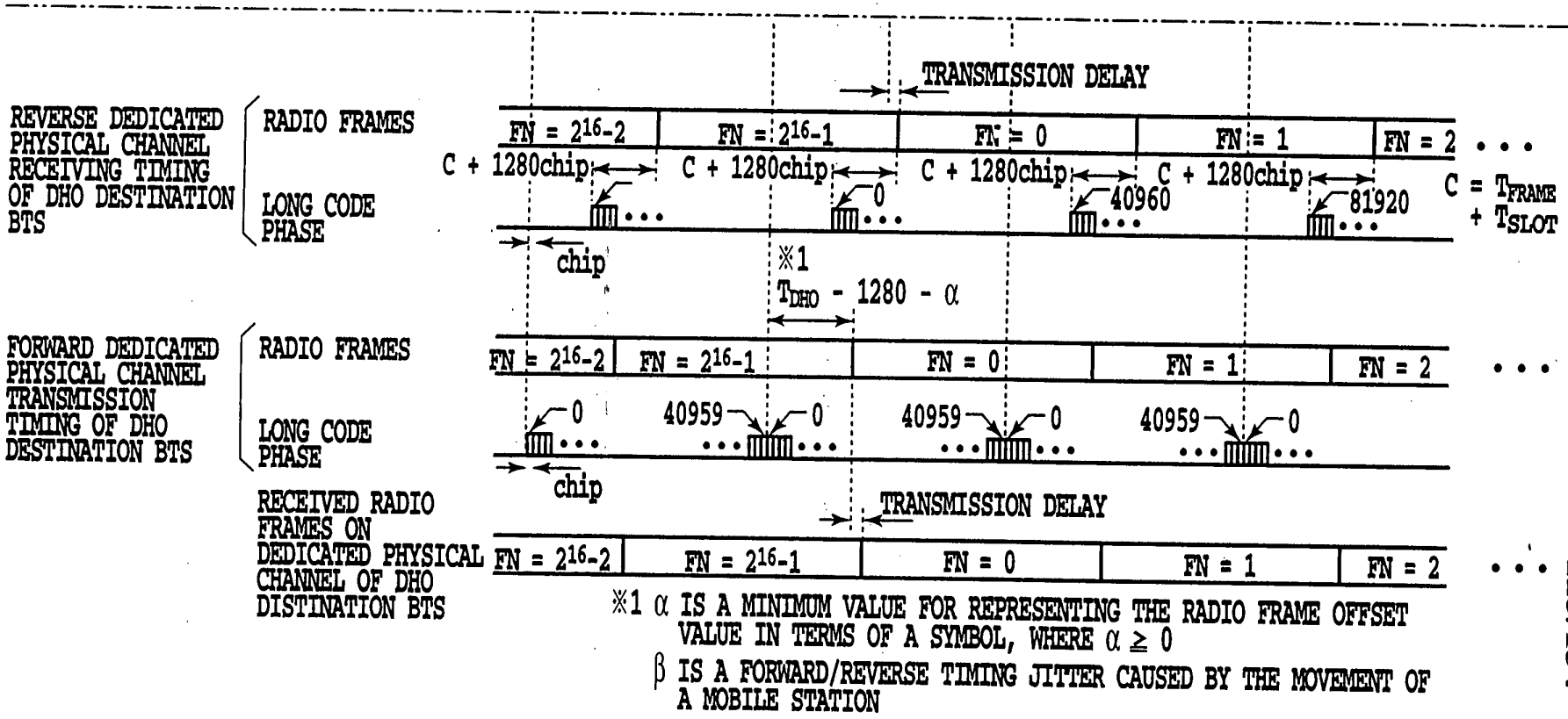

TRANSMISSION DELAY
REVERSE DEDICATED PHYSICAL CHANNEL RECEIVING TIMING OF DHO DESTINATION BTS
RADIO FRAMES
FN = 2^16-2
FN = 2^16-1
FN = 0
FN = 1
FN = 2
C + 1280chip
LONG CODE PHASE
0
40960
81920
C = T_FRAME + T_SLOT
chip
※1
T_DHO - 1280 - α
FORWARD DEDICATED PHYSICAL CHANNEL TRANSMISSION TIMING OF DHO DESTINATION BTS
RADIO FRAMES
LONG CODE PHASE
40959
chip
RECEIVED RADIO FRAMES ON DEDICATED PHYSICAL CHANNEL OF DHO DISTINATION BTS
TRANSMISSION DELAY
※1 α IS A MINIMUM VALUE FOR REPRESENTING THE RADIO FRAME OFFSET VALUE IN TERMS OF A SYMBOL, WHERE α ≧ 0
β IS A FORWARD/REVERSE TIMING JITTER CAUSED BY THE MOVEMENT OF A MOBILE STATION

FIG.88B

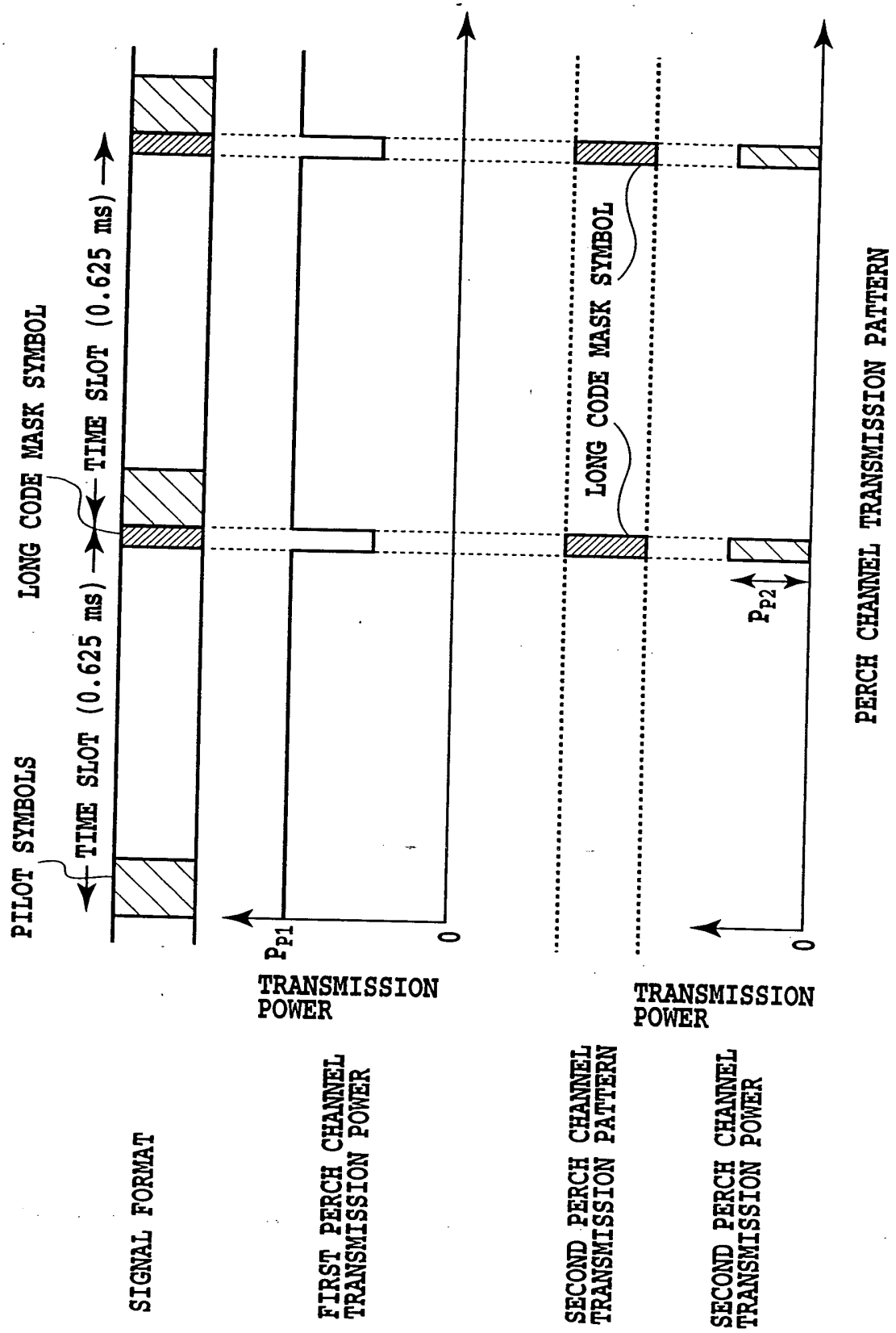

PILOT SYMBOLS
LONG CODE MASK SYMBOL
TIME SLOT (0.625 ms)
TIME SLOT (0.625 ms)
LONG CODE MASK SYMBOL
P_{P1}
0
P_{P2}
0
TRANSMISSION POWER
TRANSMISSION POWER
SIGNAL FORMAT
FIRST PERCH CHANNEL TRANSMISSION POWER
SECOND PERCH CHANNEL TRANSMISSION PATTERN
SECOND PERCH CHANNEL TRANSMISSION POWER
PERCH CHANNEL TRANSMISSION PATTERN

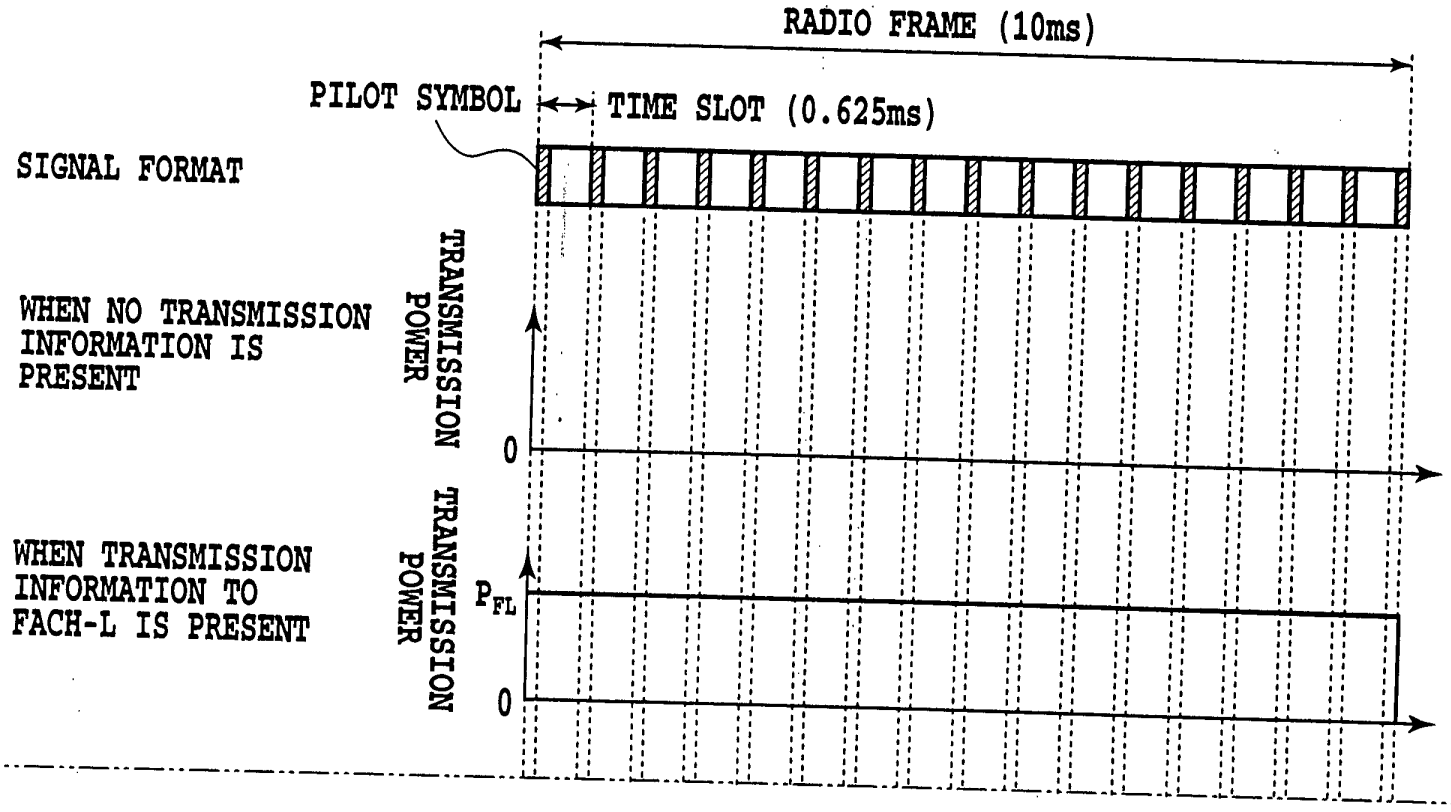
FIG.89

FIG.90

FIG.90A

FIG.90B

FIG.90A



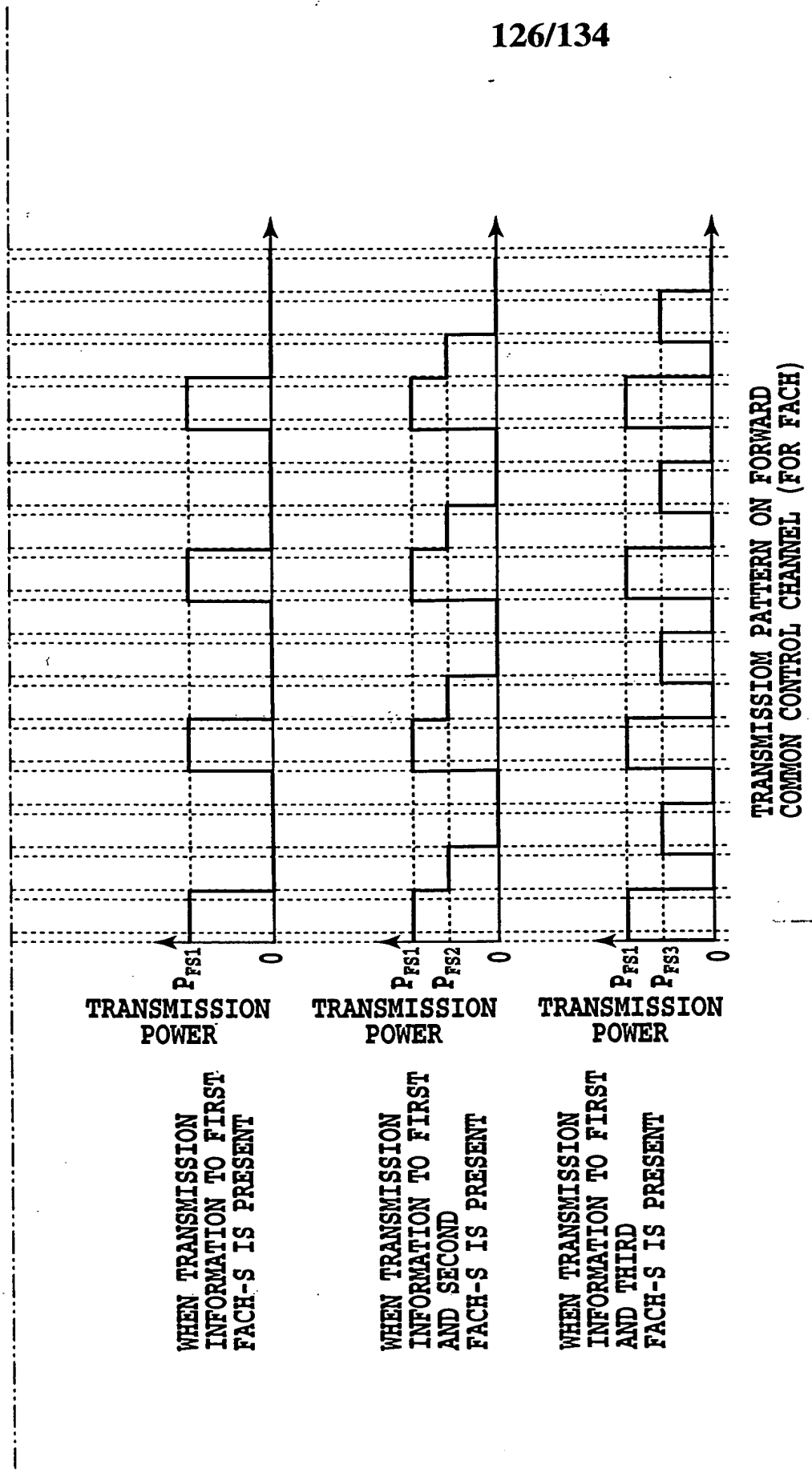

TRANSMISSION PATTERN ON FORWARD COMMON CONTROL CHANNEL (FOR FACH)
TRANSMISSION POWER
P_{FS1}
0
WHEN TRANSMISSION INFORMATION TO FIRST FACH-S IS PRESENT
TRANSMISSION POWER
P_{FS1}
P_{FS2}
0
WHEN TRANSMISSION INFORMATION TO FIRST AND SECOND FACH-S IS PRESENT
TRANSMISSION POWER
P_{FS1}
P_{FS3}
0
WHEN TRANSMISSION INFORMATION TO FIRST AND THIRD FACH-S IS PRESENT

FIG.90B

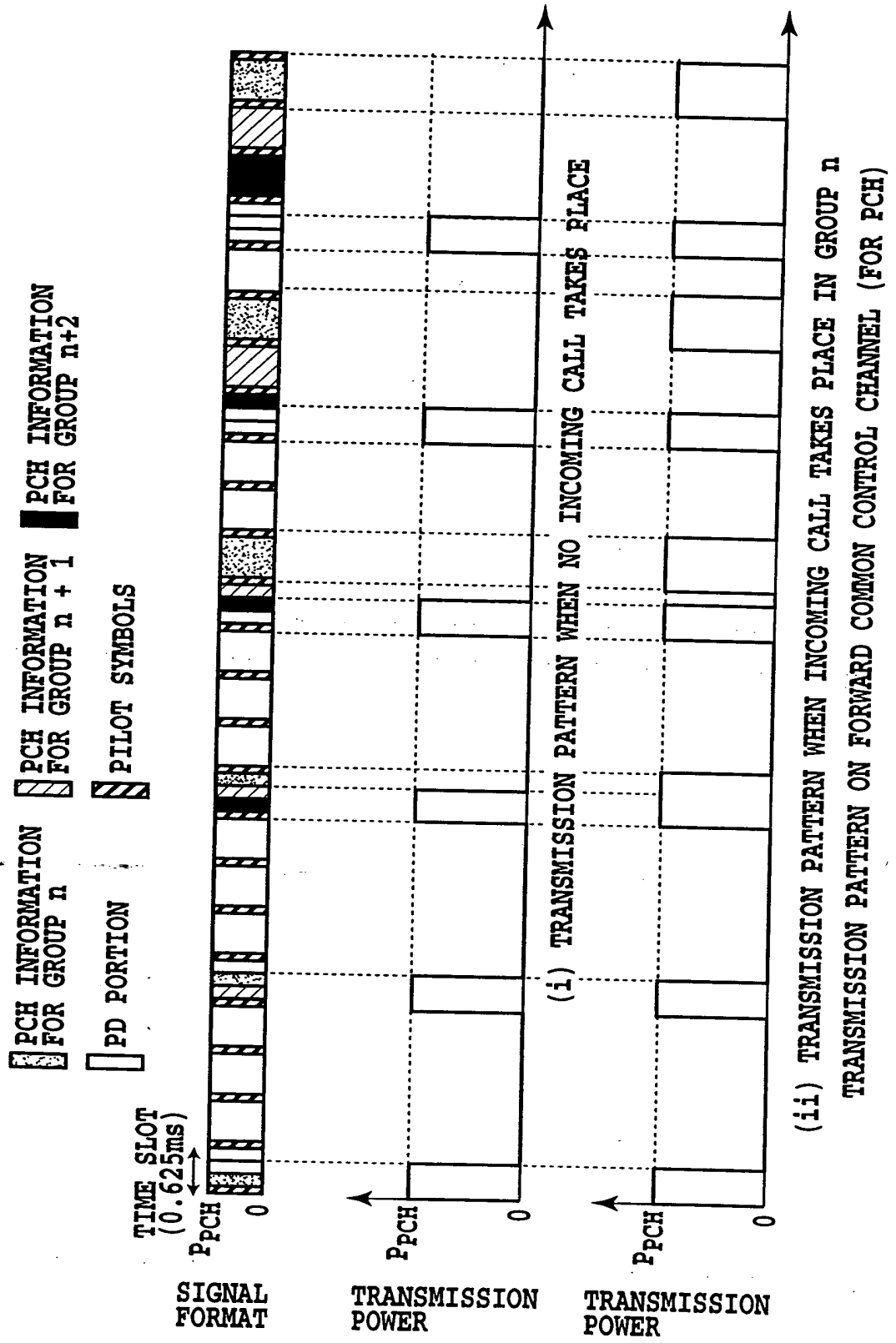

PCH INFORMATION FOR GROUP n
PD PORTION
PCH INFORMATION FOR GROUP n + 1
PILOT SYMBOLS
PCH INFORMATION FOR GROUP n+2
TIME SLOT (0.625ms)
P_{PCH}
0
SIGNAL FORMAT
(i) TRANSMISSION PATTERN WHEN NO INCOMING CALL TAKES PLACE
TRANSMISSION POWER
(ii) TRANSMISSION PATTERN WHEN INCOMING CALL TAKES PLACE IN GROUP n
TRANSMISSION PATTERN ON FORWARD COMMON CONTROL CHANNEL (FOR PCH)
TRANSMISSION POWER

FIG.91

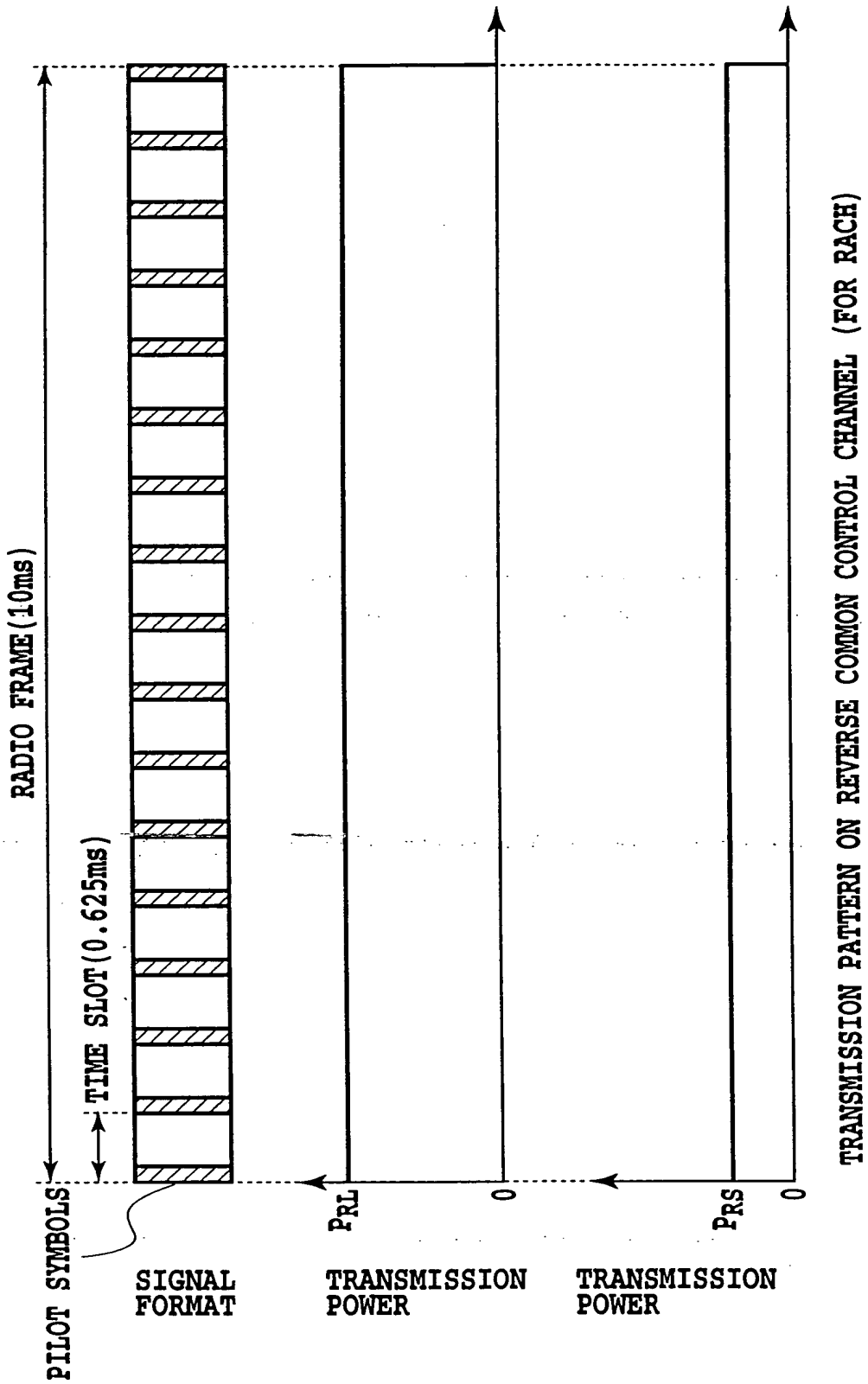

RADIO FRAME(10ms)
TIME SLOT(0.625ms)
PILOT SYMBOLS
SIGNAL FORMAT
TRANSMISSION POWER
TRANSMISSION POWER
PRL
0
PRS
0
TRANSMISSION PATTERN ON REVERSE COMMON CONTROL CHANNEL (FOR RACH)

FIG.92

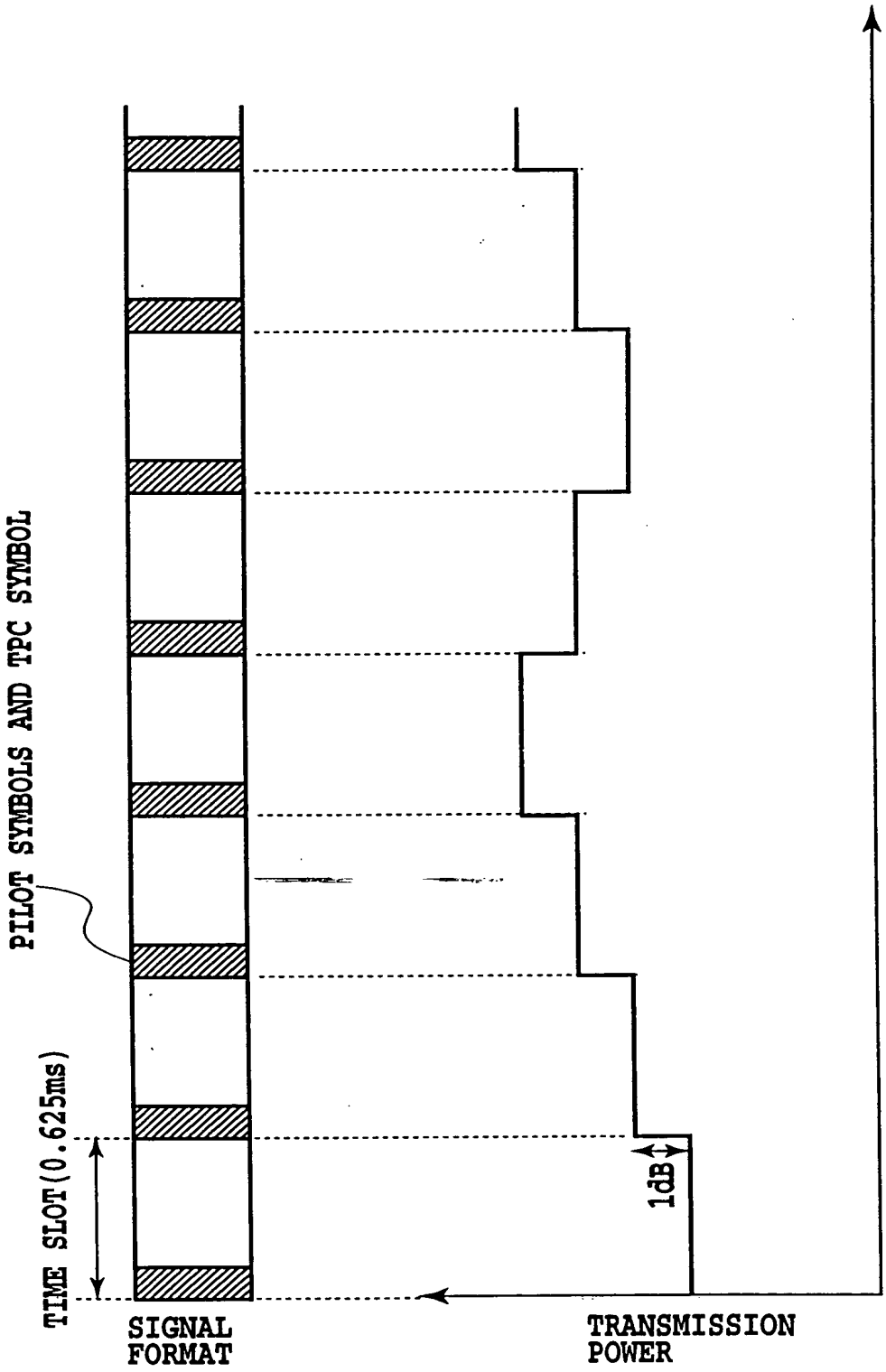
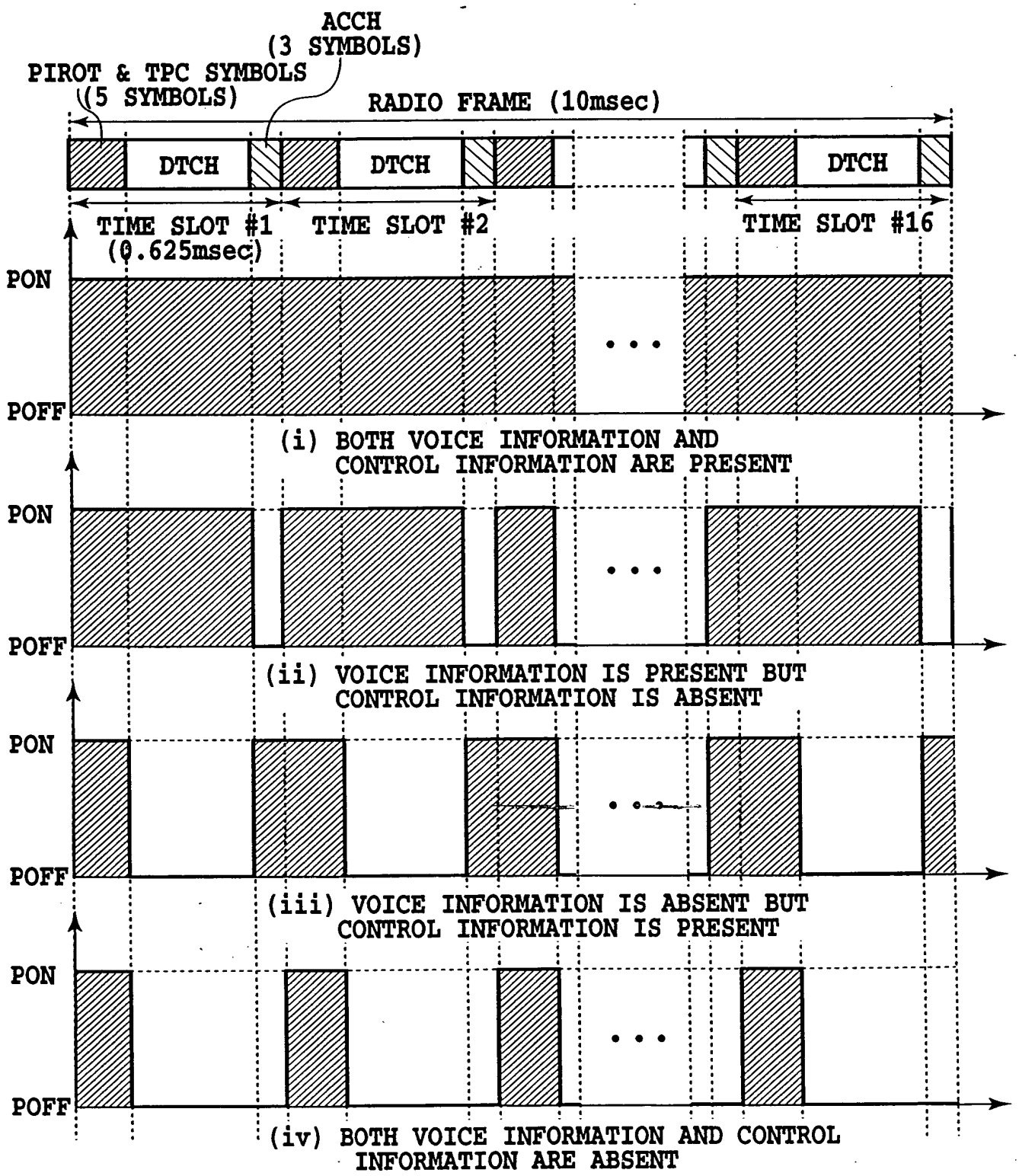

PILOT SYMBOLS AND TPC SYMBOL
TIME SLOT(0.625ms)
SIGNAL FORMAT
1dB
TRANSMISSION POWER
DEDICATED PHYSICAL CHANNEL (DURING HIGH SPEED CLOSED LOOP TRANSMISSION POWER CONTROL)

FIG.93



32 KSPS DEDICATED PHYSICAL CHANNEL (DTX CONTROL)

FIG.94

FIG.95

FIG.95A

FIG.95B

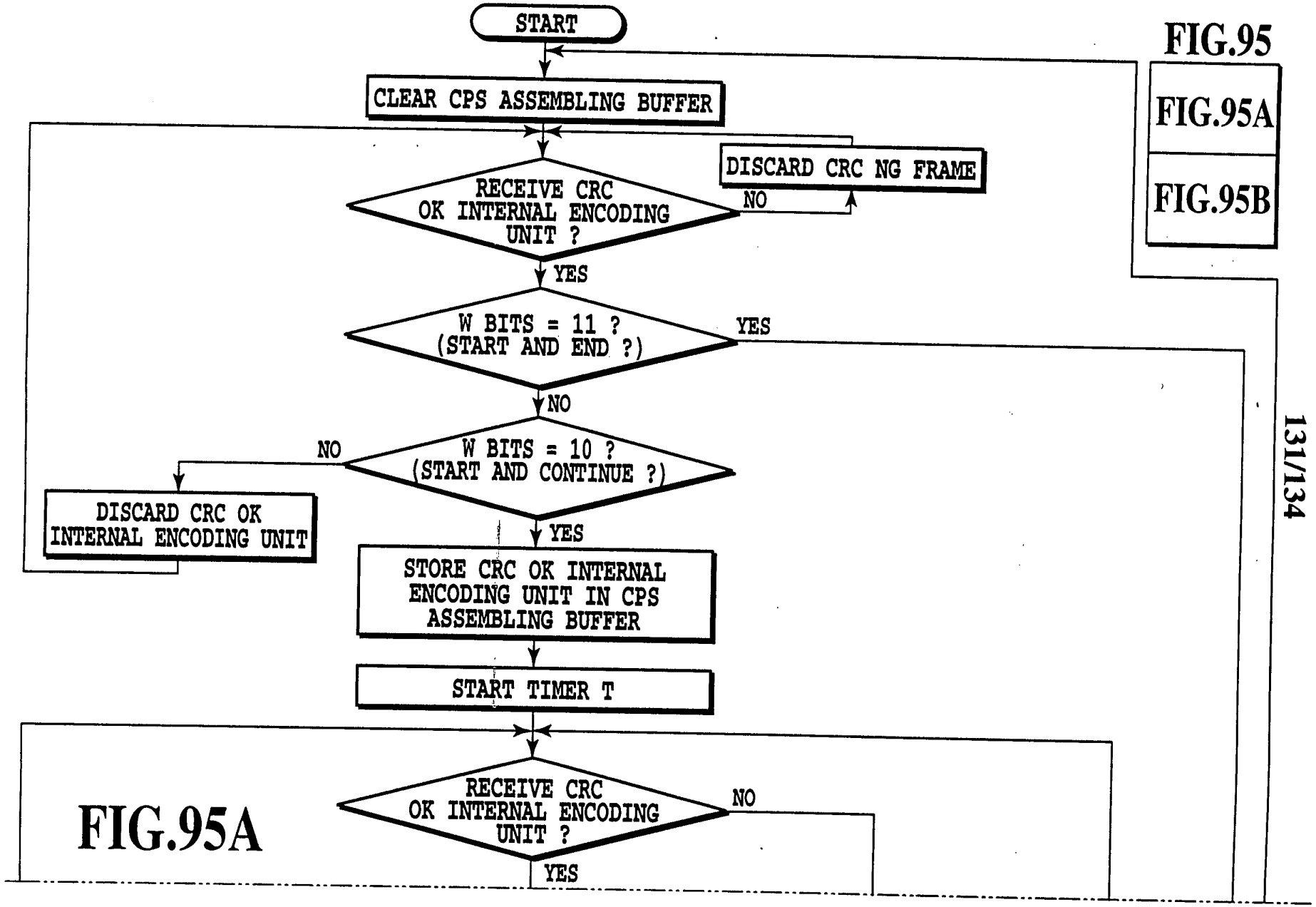


FIG.95A

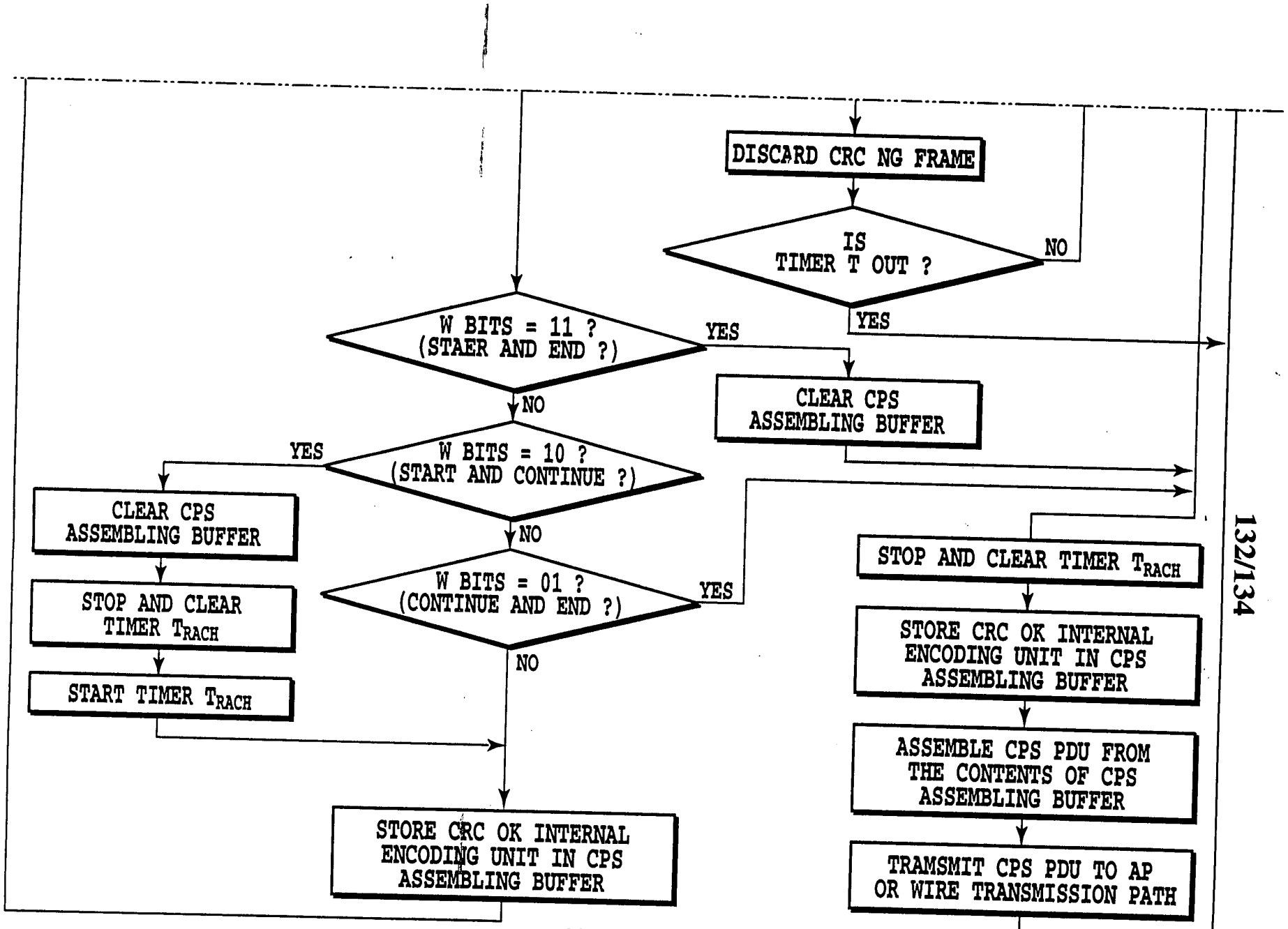

DISCARD CRC NG FRAME
IS TIMER T OUT ?
NO
YES
W BITS = 11 ? (STAER AND END ?)
YES
CLEAR CPS ASSEMBLING BUFFER
NO
W BITS = 10 ? (START AND CONTINUE ?)
YES
CLEAR CPS ASSEMBLING BUFFER
STOP AND CLEAR TIMER T_{RACH}
START TIMER T_{RACH}
NO
W BITS = 01 ? (CONTINUE AND END ?)
YES
NO
STOP AND CLEAR TIMER T_{RACH}
STORE CRC OK INTERNAL ENCODING UNIT IN CPS ASSEMBLING BUFFER
ASSEMBLE CPS PDU FROM THE CONTENTS OF CPS ASSEMBLING BUFFER
TRAMSMIT CPS PDU TO AP OR WIRE TRANSMISSION PATH
STORE CRC OK INTERNAL ENCODING UNIT IN CPS ASSEMBLING BUFFER

FIG.95B

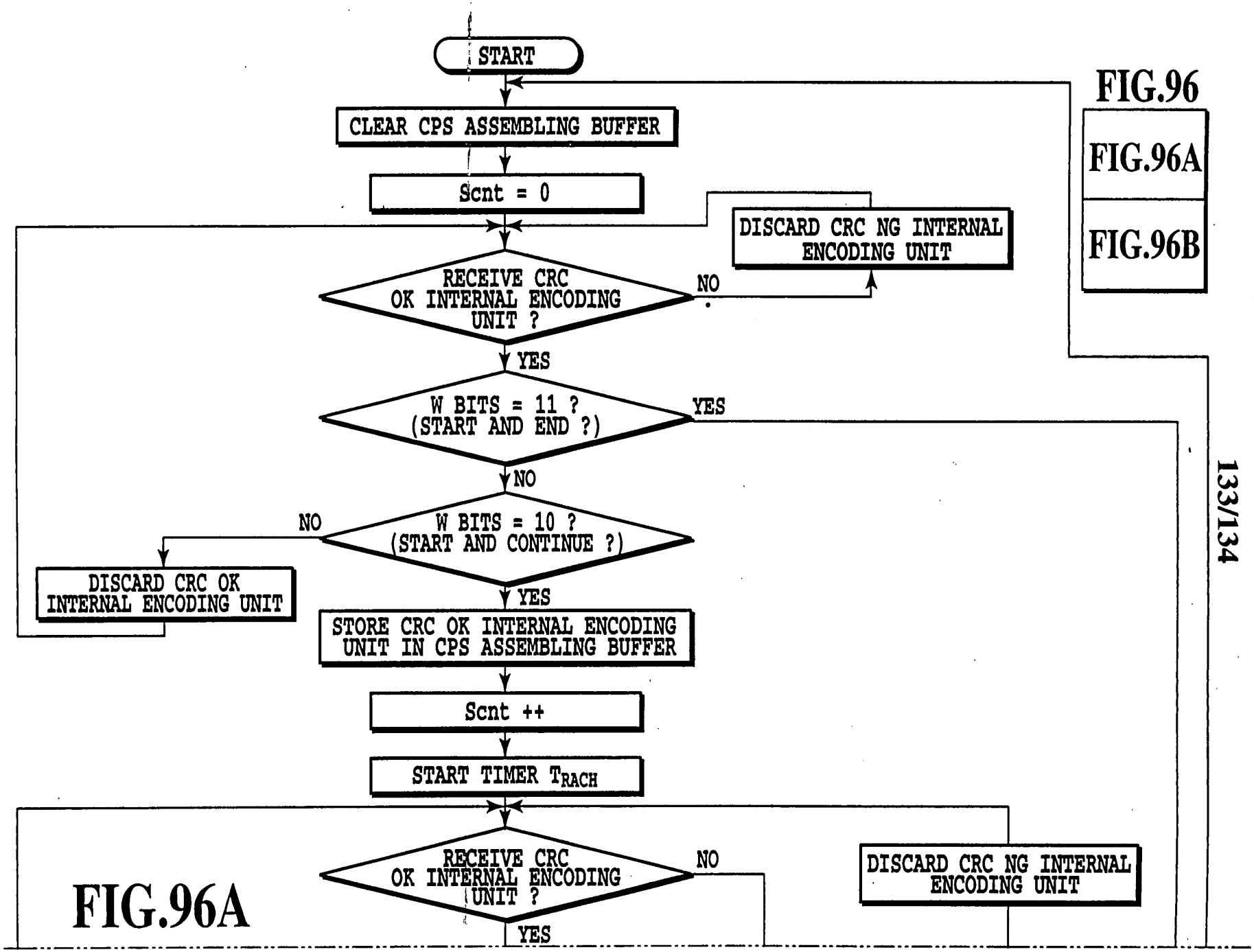


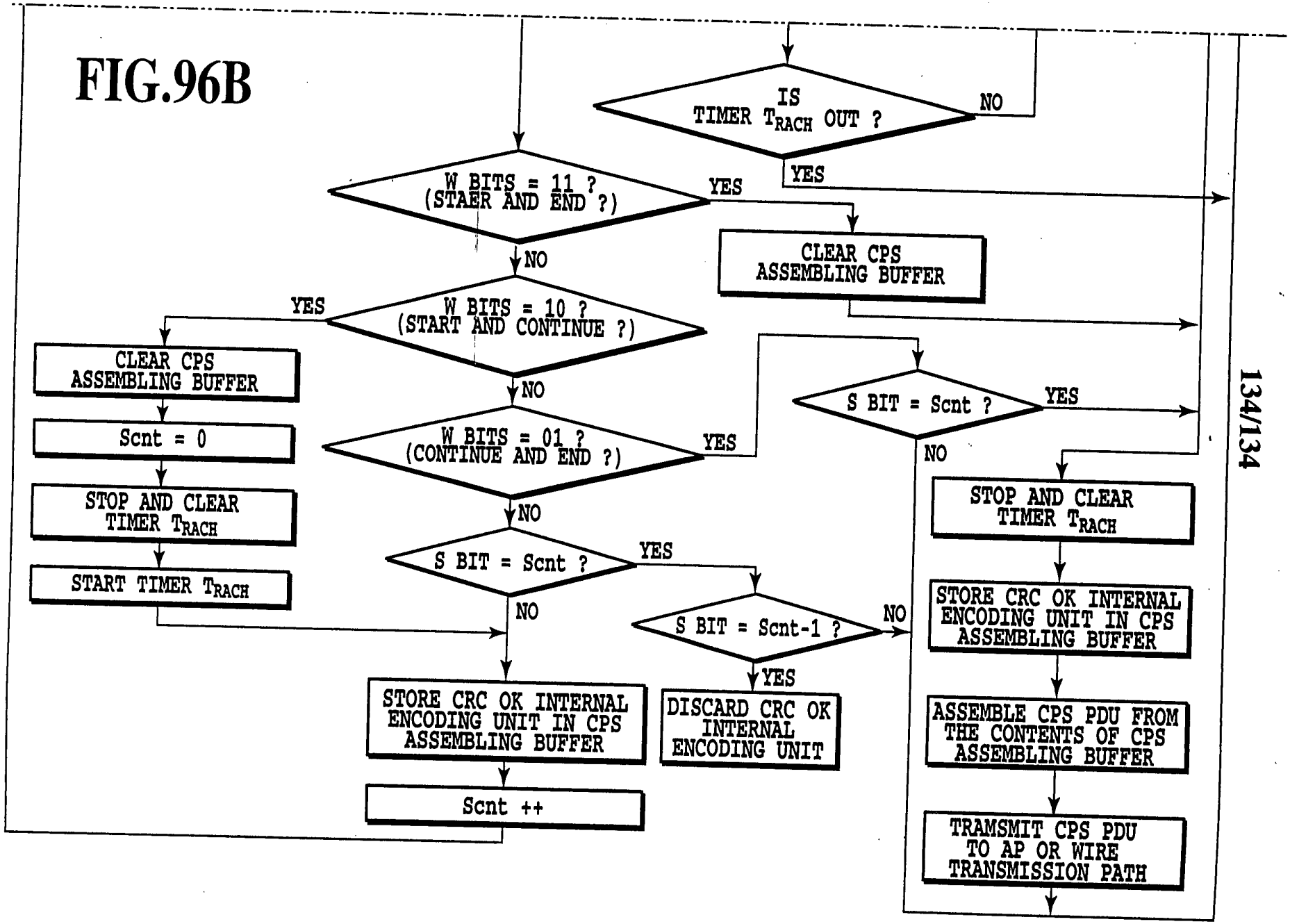
FIG.96

FIG.96A

FIG.96B

FIG.96A

FIG.96B


IS TIMER T_{RACH} OUT ?
NO
YES
W BITS = 11 ? (STAER AND END ?)
YES
CLEAR CPS ASSEMBLING BUFFER
NO
W BITS = 10 ? (START AND CONTINUE ?)
YES
CLEAR CPS ASSEMBLING BUFFER
Scnt = 0
STOP AND CLEAR TIMER T_{RACH}
START TIMER T_{RACH}
NO
W BITS = 01 ? (CONTINUE AND END ?)
YES
NO
S BIT = Scnt ?
YES
NO
S BIT = Scnt-1 ?
NO
YES
STORE CRC OK INTERNAL ENCODING UNIT IN CPS ASSEMBLING BUFFER
Scnt ++
DISCARD CRC OK INTERNAL ENCODING UNIT
S BIT = Scnt ?
YES
NO
STOP AND CLEAR TIMER T_{RACH}
STORE CRC OK INTERNAL ENCODING UNIT IN CPS ASSEMBLING BUFFER
ASSEMBLE CPS PDU FROM THE CONTENTS OF CPS ASSEMBLING BUFFER
TRAMSMIT CPS PDU TO AP OR WIRE TRANSMISSION PATH